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**DESIGN, FABRICATION AND TESTING OF P-CHANNEL ENHANCEMENT
MODE TRANSISTORS**

By

Usha R. Gowrishetty

**A Thesis
Submitted to the Faculty of the
Graduate School of the University of Louisville
In Partial Fulfillment of the Requirements
for the degree of**

Master of Science

**Department of Electrical Engineering
University of Louisville
Louisville, Kentucky**

May 2004

DESIGN, FABRICATION AND TESTING OF P-CHANNEL
ENHANCEMENT MODE TRANSISTORS

By

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A Thesis Approved on

Nov 11, 2003

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ABSTRACT

DESIGN, FABRICATION AND TESTING OF P-CHANNEL ENHANCEMENT MODE TRANSISTORS

Usha Gowrishetty

November 11, 2003

A process for fabricating PMOS transistors and test devices has been developed for educational purposes as part of a microfabrication undergraduate/graduate laboratory course at the University of Louisville. This is to help students from multiple disciplines to understand and perform basic microfabrication processes. Several designs of PMOS devices were fabricated using standard processes such as oxidation, photolithography, diffusion, and sputtering. Process characterization involved testing PMOS transistors, Cross Bridge Kelvin Structures, and Van der Pauw structures. Characterization of PMOS transistors was performed using I-V curves for varying oxide thicknesses (t_{ox}) grown using dry oxidation, wet oxidation and RTP (rapid thermal processing). Threshold voltages ranged from 1 volt for the thin RTP gate oxide to over 4 volts for the thicker gate oxide. Threshold voltages (V_{th}) were also compared to the theoretical values. Van der Pauw structures were used to determine sheet resistance (R_s) & Cross Bridge Kelvin structures for determining contact resistance (R_c). Effects on MOS-capacitors, due to gate oxide thickness, band bending with varying gate voltage and how these factors effect the functioning of transistors have been explained with the results of the fabricated devices.

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Chapter I

INTRODUCTION

A Field effect phenomenon is the basis for all modern solid-state devices. J. E. Lilienfeld and O. Heil made the first structure which resembled a transistor between 1920 and 1930, and the field effect phenomena has been derived from this structure [**Robert F. Pierret, p.1**]. This phenomena states that when a voltage is applied to a metallic plate it causes a change in the conductivity of the semiconductor which in turn changes the current flowing between the contacts A & B as shown in the Figure 1. This phenomenon of varying the conductivity of the semiconductor by applying an electric field normal to the semiconductor surface is defined as “the field effect” [**Robert F. Pierret, p.1**].

The first transistor, the bipolar junction transistor, was developed in the late 1940s and 1950s. It took years before the first modern day field-effect device, the junction field-effect transistor, was developed in the year 1952 [**Robert F. Pierret, p.1**]. This led to the development of the metal-oxide field effect transistors in the later years. Initially the development in the semiconductor industry was stagnated due to lack of modern day technology. Today semiconductor industry is a \$300B industry which fabricates semiconductor devices in huge volumes. Commercial industries which develop semiconductor

devices include Fairchild Semiconductor, Honeywell, and Intel. Semiconductor devices are useful in every moment of the existence of human life.

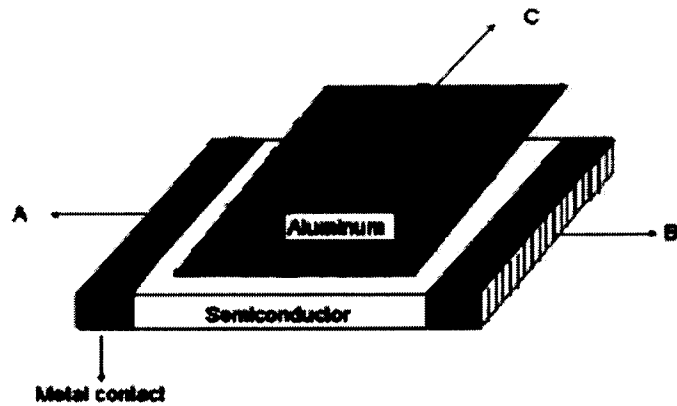


Figure 1 Illustration of the first FET phenomena [Robert F. Pierret, p.1]

Chapter II

DESIGN & THEORY

2.1 Design

A four mask process was designed for the fabrication of PMOS transistors. The dimensions of the mask design have a great affect on the characteristics of the fabricated structures. The masks designed for the fabrication of the PMOS transistors are shown in Appendix A. The boron diffusion mask is used for determining the doping region. The gate oxide mask is used for opening windows in the field oxide for growing the thin gate oxide. The contact window mask is used to open contact windows in the oxide for making contacts to the diffused regions. The metallization mask is used for making metal contacts to the diffused regions and creating the gate. Design dimensions that affect the functioning of the PMOS transistors are gate oxide thickness, channel length and the channel width.

Transistors with channel length less than $1\mu\text{m}$ are said to be short channel transistors [Robert F. Pierret, p.137-138]. Short channels help in miniaturization of the devices by fitting more transistors in a given area. If the short channel transistors are fabricated without proper care it will result in leakage currents or tunneling currents between the source and the drain. These will in-turn affect the turn-on voltage of the transistor. In this case, it will result in a lesser value of the turn-on voltage. Therefore, the channel lengths should not be made too small if

the conditions in the cleanroom are not appropriate. Also, the electrical characteristics of the short channel devices are more complex and are modeled by a modified set of equations. In this research we focus on long channel devices.

Affects of variation in the channel width and gate oxide thickness are given below. If the width of the channel increases, the conductance of the channel increases reducing the resistance of the transistor. Gate oxide thickness affects the turn-on voltage of the transistor. Reduction in the gate oxide thickness lowers the turn-on voltage. The transistors which we fabricated are all long channel transistors, since the length of the channel is greater than 1 μ m and also longer than the width of the channel. We have different gate oxide thicknesses for the transistors we fabricated. Design specifications for the transistors we fabricated are given in Table 1.

Table 1 Channel length and width of the transistors

Channel Length(μ m)	Channel Width(μ m)
40	40
60	40
80	40
20	100

2.2 Theory

MOS transistors can be of two types, that is, enhancement mode and depletion mode. Enhancement mode and depletion mode are related to the channel between the source and the drain. If the channel exists between the source and the drain before applying any voltage between the gate and the substrate, the transistor is said to be operating in depletion mode. When no channel exists between the source and the drain, and the voltage between the gate and the substrate is zero, the transistor is said to be operating in enhancement mode.

Apart from the enhancement and depletion modes, the transistor can be operated in either the cutoff region, linear region or saturation region depending on the voltage V_{ds} and the current I_{ds} . These operating regions of the transistor are explained in Section 2.2.6. MOS-capacitors play an important role in the performance of the transistor operation. It is the MOS-capacitor which lies between the source and the drain and in which the channel is formed that determines if the transistor is operating in enhancement or depletion mode. MOS-capacitors also help in determining the charges in the gate oxide. A MOS-capacitor connected to the C-V instrument is left undisturbed for a few hours and if a shift occurs in the C-V curve, it is understood that there are some charges in the gate oxide.

2.2.1 MOS-Capacitor

The MOS-capacitor is a simple two terminal device considered to be the heart of the PMOS transistor. A thin layer of the oxide on the surface of the

semiconductor acts as the dielectric. The metal contact made on the oxide layer and the silicon substrate act as the two plates of the capacitor as shown in Figure 2. The contact made to the oxide layer is known as the gate for the MOS transistors. For a PMOS-transistor, applying a negative bias between the gate and the semiconductor causes the inversion layer [Robert F. Pierret, p.29-30, Ben G Streetman & Sanjay Banerjee, p.260].

Properties of the MOS-capacitors vary for ideal and non-ideal gate oxide. Ideal MOS-capacitor is considered to have an oxide layer with no charge centers (mobile charges, interfacial traps, and oxide trapped charges) and the oxide layer acts as a perfect insulator [Robert F. Pierret, p-32]. A band diagram of an ideal MOS-capacitor is shown in Figure 3 [Ben G Streetman & Sanjay Banerjee, p.267-269, Nicollian Brews, p.65]. The band bending and charge diagrams for varying biasing conditions across the MOS-capacitor are explained in Section 2.2.8.

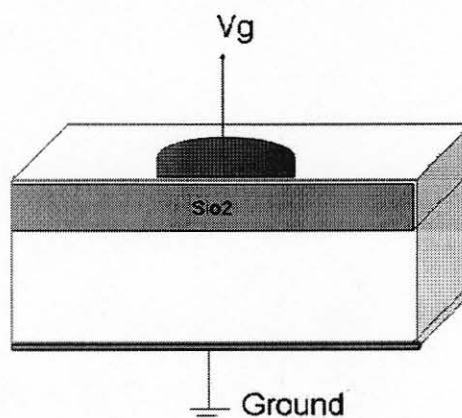


Figure 2 MOS-capacitor [Robert F. Pierret, p.30]

2.2.2 Distribution of the Gate Voltage

The MOS structure is considered to be at equilibrium when $V_g=0$ and the Fermi energy levels are in line with each other as shown in Figure 3. For creating the inversion layer, one applies a voltage $V_g < 0$ & $V_g = V_{th}$ between the two plates of the capacitor. V_{th} is known as the threshold voltage. The voltage applied is dropped across the gate oxide and the semiconductor, which appear in series with each other. The voltage dropped across the gate oxide is utilized in acquiring the charges on the semiconductor surface for balancing the negative charge on the metal surface. The voltage dropped across the semiconductor substrate is utilized in creating the inversion layer. This is known as the surface potential ϕ_s , as shown in Figure 4 [Ben G Streetman & Sanjay Banerjee, p.267-269, Nicollian Brews, p.65].

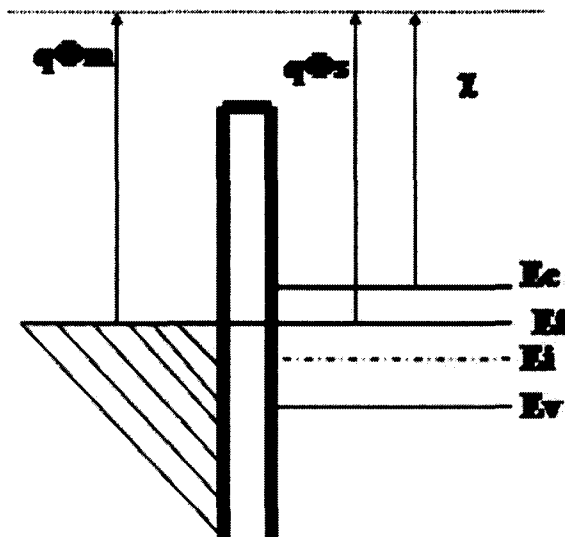


Figure 3 Ideal MOS structure [Robert F. Pierret, p.32]

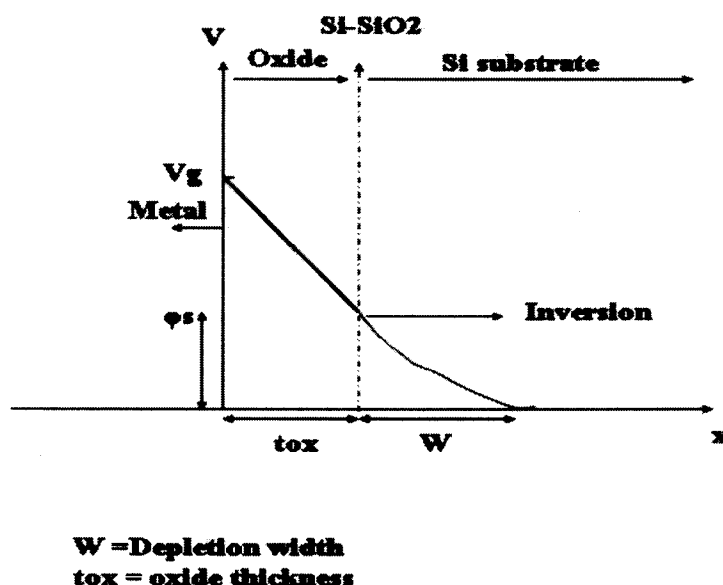


Figure 4 Voltage drop across the oxide and semiconductor [Nicollian Brews, p.65]

For a non-ideal MOS-capacitor the threshold voltage will have an additional term. This additional term is used in attaining the flat band condition as shown in Figure 5. Voltage required in overcoming the oxide charges in the gate oxide and the work function difference between the metal and the semiconductor is known as the flat band voltage [Ben G Streetman & Sanjay Banerjee, p.272-277].

2.2.3 Threshold Voltage

The Voltage required to create the inversion layer at the Si-SiO₂ interface is known as the threshold voltage. The threshold voltage for an ideal MOS-capacitor is given by equation 1 [Ben G Streetman & Sanjay Banerjee, p.260-

269,275, S. M. Sze, p.199-210] and voltage required for creating the inversion is given by equation 2. MathCAD solutions for threshold voltage of varying gate oxide thickness from different processes wet oxidation, dry oxidation and RTP are given in the Appendix B. Comparison between practical and theoretical values of threshold voltage is dealt in Section 4.4.

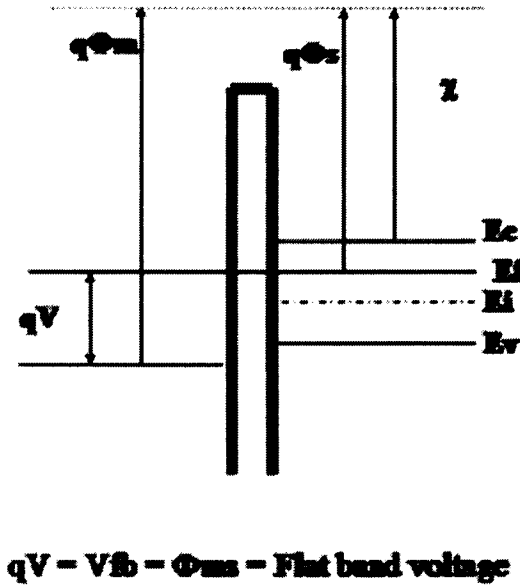


Figure 5 MOS structure with flat band voltage [Robert F. Pierret, p.36]

$$V_{th} = \frac{Q_{ox}}{C_{ox}} - \phi_s \quad (\text{Ideal Case}) \quad (1)$$

V_{th} = Threshold voltage (Volts)

ϕ_s = Voltage required in creating the inversion (Volts)

$$\phi_s = 2\phi_f = \frac{kT}{q} \ln \frac{N_b}{n_i} \quad (2)$$

$\frac{Q_{ox}}{C_{ox}}$ = Voltage across the ideal gate oxide (Volts)

N_b = Background concentration ($1/\text{cm}^3$)

n_i = Intrinsic concentration ($1/\text{cm}^3$)

C_{ox} = Gate oxide capacitance (Farad)

Q_{ox} = Charge due to depletion on the gate oxide (Farad)

The threshold voltage for a non-ideal MOS-capacitor is given by equation 3

$$V_{th} = \frac{Q_{ox}}{C_{ox}} - \phi_s + \left[\Phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} \right] \text{ (Non-ideal case)} \quad (3)$$

$$V_{fb} = \Phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} \quad (4)$$

V_{fb} = Voltage required in achieving the flat band condition (Volts)

Q_f = Oxide fixed charge (Farad)

Q_m = Mobile ionic charge (Farad)

Q_{ot} = Oxide trap charge (Farad)

Φ_{ms} = Metal semiconductor work function difference (Volts)

Definitions of the work function, electron affinity, barrier height and inversion layer are explained below:

1. Work function (Φ_m, Φ_s)

The energy difference between vacuum level and Fermi energy level (E_f) in a metal is known as the metal work function (Φ_m). Similarly energy difference between vacuum level and Fermi energy level (E_f) in the

semiconductor is known as the semiconductor work function (Φ_s) [Ben G Streetman & Sanjay Banerjee, p.220-221].

2. Electron affinity (χ)

Energy difference between the conduction band and the vacuum level is known as the electron affinity (χ) [Ben G Streetman & Sanjay Banerjee, p.220-221].

3. Barrier Height (ϕ_b)

The difference between the metal work function and electron affinity is known as the barrier height [Ben G Streetman & Sanjay Banerjee, p.220-221]. Equation for the barrier height is given as

$$\phi_b = \Phi_m - \chi \quad (5)$$

ϕ_b = Barrier Height (Volts)

Φ_m = Metal work function (Volts)

χ = Electron affinity (electron volts)

4. Inversion Layer

Transition from n-type region to p-type region or vice versa at the Si-SiO₂ interface is known as inversion [Ben G Streetman & Sanjay Banerjee, p.220-221]. The inversion layer is formed at the Si-SiO₂ interface. The inversion layer is a result of the depletion of the majority carriers (Depends on the substrate dopant type. Majority carriers are electrons for n-type and holes for p-type) from the interface and aggregation of the minority carriers (Depends on diffused regions dopant type. Electrons for phosphorus diffusion and holes for boron diffusion) at the interface when

a voltage is applied across the gate. Thus, the inversion layer consists of minority carriers. This layer is otherwise known as the channel between the source and the drain.

For the inversion layer to remain in between the source and the drain there need not be any motion in the carriers or the charges. With no drain to source voltage, the existence of the inversion layer only depends on the gate voltage. When the drain to source voltage is applied, the voltage across the channel varies. This might result in breaking the channel thus causing pinch-off to occur. So, the voltage between the gate and the substrate must be greater than or equal to the threshold voltage to sustain the channel. This voltage is the minimum voltage to maintain the channel. The inversion layer is very important for the functioning of the transistors.

2.2.4 Gate oxide charges

Charges in the gate oxide are introduced apparently during the oxidation process due to any contamination in the furnace, wafer boat, inserting rod or contamination in the cleanroom itself. These charges in the gate oxide result in shifts in the turn-on voltage and variation for capacitance across the gate oxide with time, causing instabilities in the functioning of the transistors [**Robert F. Pierret, p.95**]. Charges captured in the gate oxide are shown in Figure 6 and are explained below.

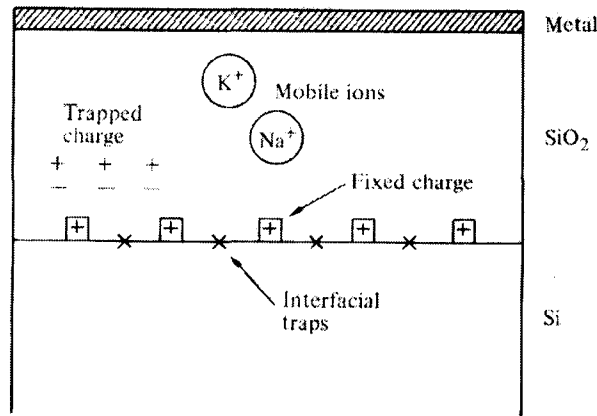


Figure 6 Location of charge centers in thermally grown Si-SiO₂ structures
[Robert F. Pierret, p.95]

2.2.4.1 Mobile ions

Mobile ions include sodium, lithium and potassium which move freely through quartz and SiO₂ at temperatures below 250°C. Of all these mobile ions, the sodium ions are the most common and are the cause for the instabilities in the performance of transistors. They are found in the quartz apparatus and wafer boats used for gate oxidation or deposition. These ions causes shift in C-V characteristics which were rectified but could not be prevented completely initially. These mobile ions affect the threshold voltage **[Robert F. Pierret, p.98]**.

Rectification of the mobile ions is explained below.

- a. Phosphorus stabilization is done by diffusing phosphorus through the oxidized wafer. This results in the formation of a thin layer of phosphosilicate glass on the surface of the SiO₂ film. At high temperatures of diffusion (1000°C), sodium ions which are extremely mobile, move into the phosphosilicate glass region and get trapped as shown in Figure 37. This process of trapping the ions is known as

gettering. The ions remain fixed in the phosphosilicate glass region even after the temperature cools down. This stabilizes the mobile ions in the gate oxide [**Robert F. Pierret, p.102**].

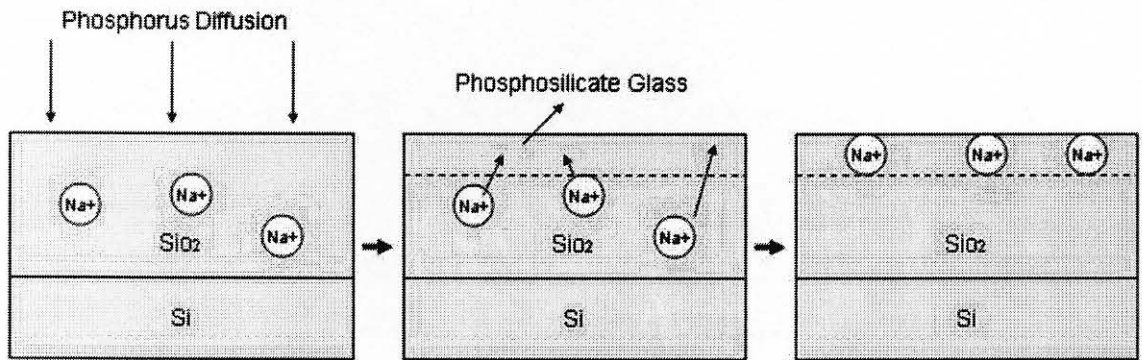


Figure 7 Phosphorus stabilization [**Robert F. Pierret, p.102**]

- b. Chlorine neutralization is done by introducing Cl₂, HCl or trichloroethane into the bubbler during the growth of SiO₂. Chlorine enters the oxide and forms chlorosiloxane at the Si-SiO₂ interface as shown in the Figure 8. The sodium ions move into the chlorosiloxane region and get trapped. The sodium ions get neutralized by the chlorine in the chlorosiloxane region. This stabilizes the mobile ions in the gate oxide [**Robert F. Pierret, p.102**].

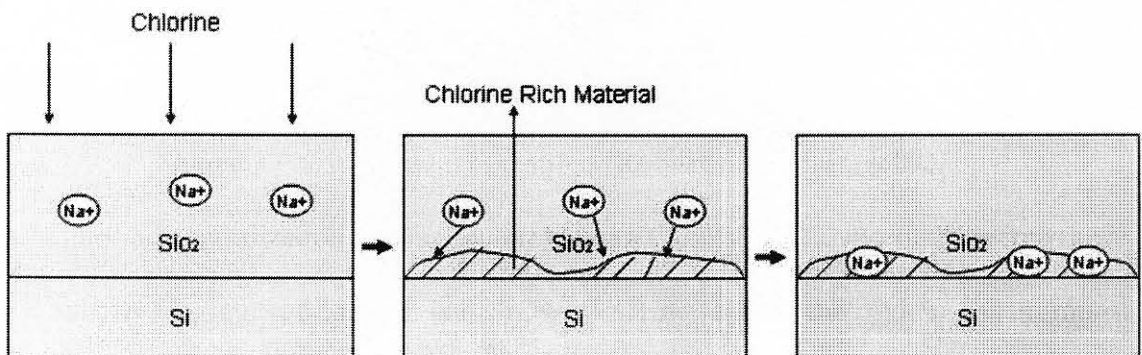


Figure 8 Chlorine neutralization [**Robert F. Pierret, p.102**]

2.2.4.2 Interfacial Traps

Interfacial traps result in the rise of the threshold voltage (gate voltage V_{gs}). When a gate voltage is applied to the transistor with interfacial traps the voltage initially is utilized in filling traps in the Si-SiO₂ interface region. Later the voltage is utilized in forming the inversion layer. This causes an increase in the threshold voltage. Rectification of the interfacial traps is explained below.

Interfacial states are allowed energy states, that is, interface states in the forbidden band gap at the Si-SiO₂ interface. These interface states are lack of electrons. Interfacial states are a result of the dangling bonds as shown in the Figure 9 [Robert F. Pierret, p.106]. Annealing is done to minimize the interfacial trap concentration and to get better contact between the metal and the silicon which is explained below.

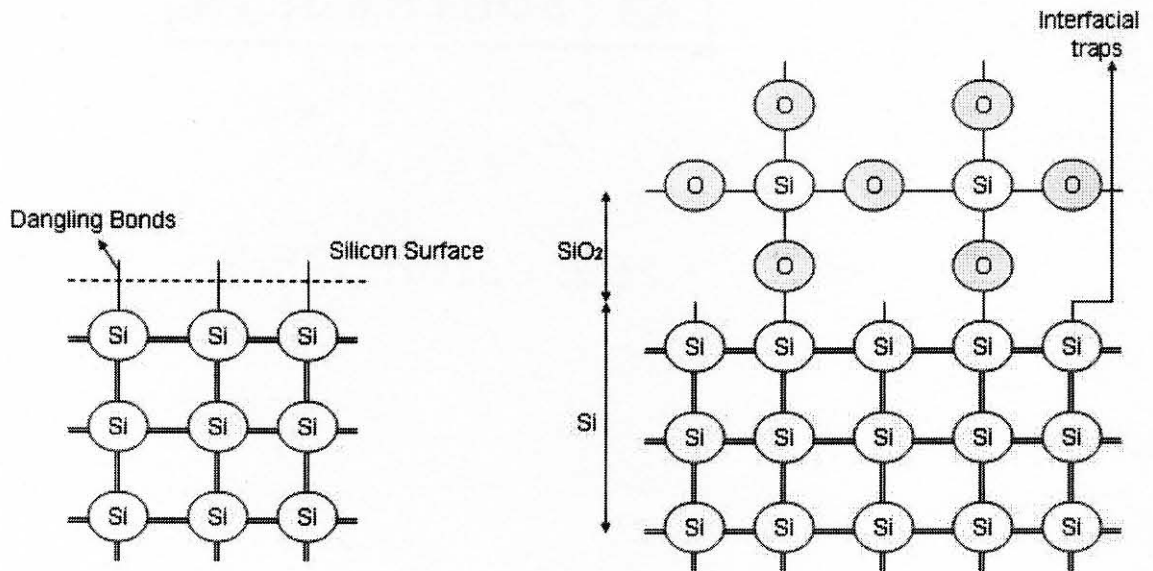


Figure 9 Dangling bonds at the silicon surface and interfacial traps seen after the oxidation process [Robert F. Pierret, p.106]

- a. During the post metallization process, the fabricated structure is placed in a nitrogen atmosphere at 450°C for 5 to 10 minutes. During annealing, the gate material reacts with the water vapor in the surface of the gate oxide and releases hydrogen atoms which form bonds with the dangling silicon bonds as shown in Figure 10. Thus annealing reduces the dangling bonds, thereby reducing the interfacial traps. Hydrogen can also be used in place of nitrogen, so that the required hydrogen atoms can be supplied directly to form bonds with the dangling silicon atoms [Robert F. Pierret, p.108-111].

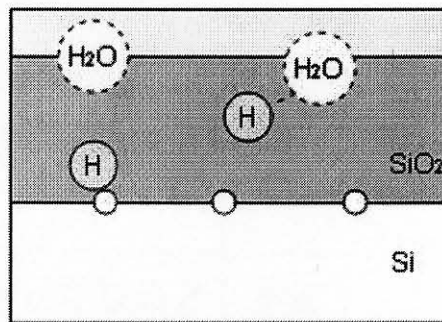


Figure 10 Hydrogen atoms reacting with the dangling bonds at the Si-SiO₂ interface [Robert F. Pierret, p.111]

- b. Annealing done in an argon atmosphere at 450°C for 15 minutes results in good contact between the silicon and the aluminum metal. Aluminum at this temperature consumes Si and forms good contact with silicon wafer. If this process is continued for a long time it might result in spikes as shown in Figure 11 which might result in a short circuit [Robert F. Pierret, p.108-111].

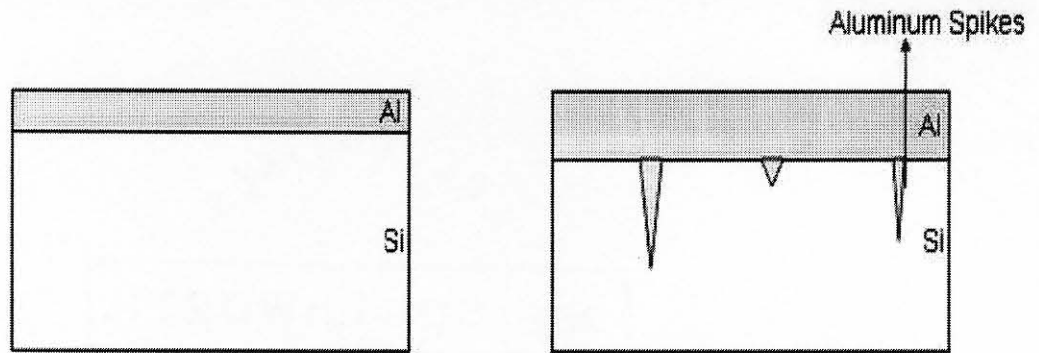


Figure 11 Formation of Al spikes with annealing for a long time [Richard P. Jaeger]

2.2.5 PMOS Basic Operation

PMOS stands for P-channel metal oxide semiconductor. PMOS transistors have a gate, drain and source region as shown in Figure 12. An enhancement mode device needs to be turned ON from an OFF state. One applies a voltage V_g across the gate to form the inversion layer. At a voltage $V_g = V_{th}$, the inversion layer is formed. Applying a reverse bias voltage V_{ds} between the drain and the source induces motion in the charges in the channel from the source to the drain. This turns the transistor ON. This process of turning the transistor ON and later the pinch-off coming into view is shown in Figure 13 [Ben G Streetman & Sanjay Banerjee, p.257]. An in depth explanation of the operating procedure of the transistors is illustrated in Section 2.2.6.

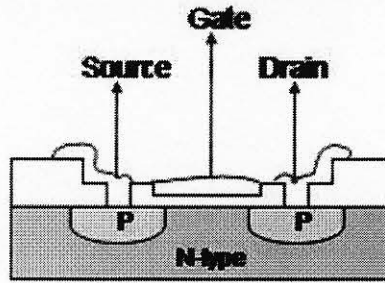


Figure 12 PMOS transistor

If the substrate is of p-type, the diffused regions would be of n-type and the channel between the source and the drain would be due to electrons that are the minority carriers. Voltage applied across the gate V_g and the drain to source voltage V_{ds} will be positive [**Ben G Streetman & Sanjay Banerjee, p.257**].

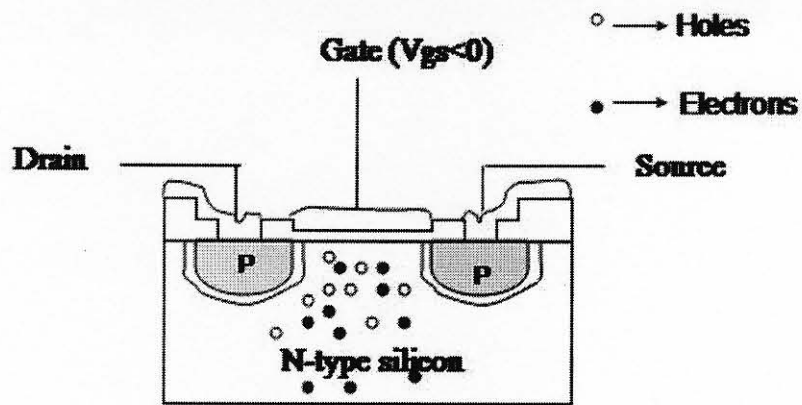
2.2.6 Operating Procedure

Principle operations of the transistors depend on the flow of electrons from the source to the drain when the gate voltage V_g and the drain voltage V_{ds} are applied across the gate and the drain respectively [**Robert F. Pierret, p.65-69, Neil H. E. Weste & Kamran Eshraghian, p.45**]. Turning the transistor ON requires the inversion layer and a negative voltage V_{ds} across the drain and the source. With no channel there is an open circuit between the source and the drain. The inversion layer is formed by applying a voltage $V_g = V_{th}$ as shown in Figure 13. The interface biasing conditions that follow are explained in detail in Section 2.2.8.

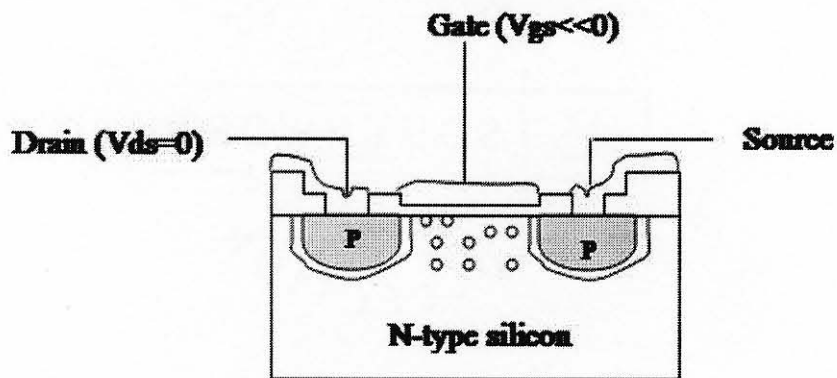
1. With the gate voltage positive ($V_g > 0$), the interface region is accumulated with the electrons.
2. With the gate voltage negative ($|V_g| < |V_{th}|$), the interface region is depleted of the electrons.
3. With the gate voltage negative ($V_g = V_{th}$), the interface region is at the onset of inversion.
4. With the gate voltage negative ($|V_g| \geq |V_{th}|$), the interface is in the inversion region [Neil H. E. Weste & Kamran Eshraghian, p-45-50].

After the formation of the inversion layer, we need to induce motion in these charges. This is achieved by applying a voltage V_{ds} between the drain and the source. Several phases of operation of the MOS-Transistors due to the regulation of the drain to the source voltage are as follows:

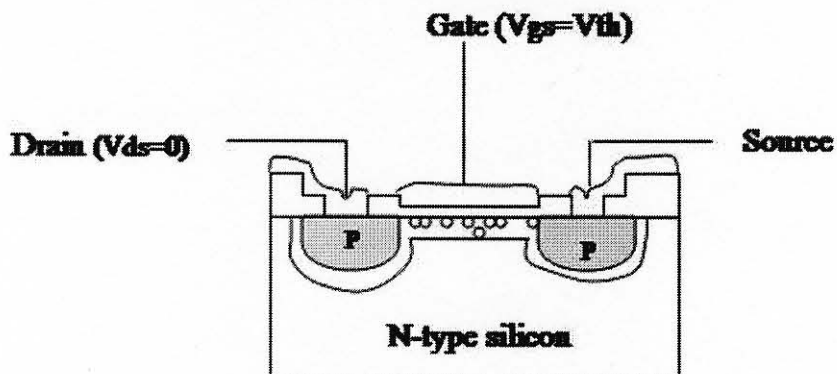
1. When $V_g > 0$, and $V_{ds} = 0$ the current $I_{ds} = 0$ between the source and the drain. The transistor is operating in the cut-off region as shown in Figure 15.
2. When $|V_{ds}| < |V_g| - |V_{th}|$, the voltage at the source end of the channel is V_g and at the drain end of the channel is $|V_d| < |V_g| - |V_{th}|$. That is $|V_d| - |V_g| > |V_{th}|$ and is adequate enough to retain the inversion layer. This voltage V_{ds} induces motion in the holes resulting in the current I_{ds} . The transistor is operating in the linear region as shown in Figure 15.



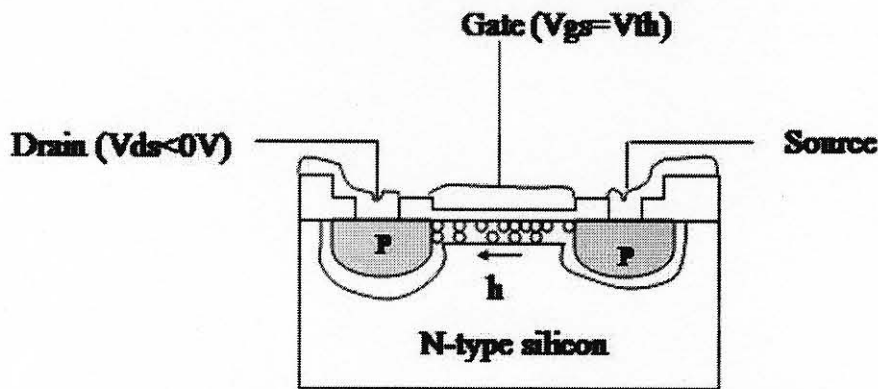
With $V_{gs} < 0$, holes moving towards the Si-SiO₂ interface & electrons moving away from the interface



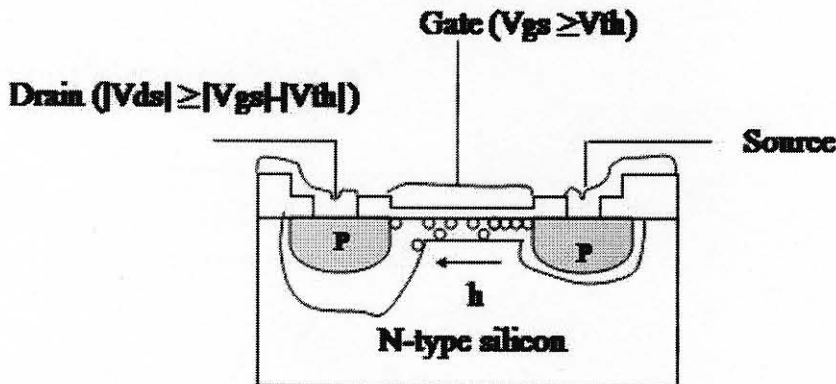
With $V_{gs} \ll 0$ holes start collecting at the interface



With $V_{gs} = V_{th}$ a p-channel is formed between the source and the drain.
 $V_{ds} = 0$ so there are no flow of electrons from the source to the drain



With $V_{gs} = V_{th}$ & $V_{ds} < 0$, the drain is reverse biased, this negative voltage attracts the holes from the source to the drain end and the channel starts conducting.



With $|V_{ds}| \geq |V_{gs}| - |V_{th}|$ holes at the drain end get depleted that is pinch off occurs and the current is known as the saturation current (holes diffuse from the point of pinch-off to the drain through the depletion region resulting in the current instead of turning the transistor OFF)

Figure 13 Various stages of the transistor with varying V_{gs} & V_{ds}

3. Increasing the drain to source voltage V_{ds} results in $|V_{ds}| \geq |V_g| - |V_{th}|$. The voltage at the source end of the channel is V_g and at the drain end of the channel is $|V_d| > |V_g| - |V_{th}|$. That is $|V_d| - |V_g| < |V_{th}|$ resulting in the voltage going below the turn-on voltage across the channel. The inversion layer

can no longer be retained. Pinch-off occurs at the drain end of the channel and the channel breaks. There is no longer a connection between the source and the drain. This does not turn the transistor OFF. The current I_{ds} still exists but remains constant. This current is due to the diffusion of the holes from the point of pinch-off to the drain. The transistor is operating in the saturation region as shown in Figure 15. The current is represented as $I_{ds(sat)}$. This process of the pinch-off occurring is shown in Figure 14.

With the voltage applied across the drain and the source, the drain is reverse biased. As the voltage is increased further, the depletion region at the drain end increases. This causes the movement of the holes away from the drain. This is one cause for the pinch-off. Another cause for the pinch-off is the voltage across the channel dropping below V_{th} . This has been explained above. Increasing the gate voltage $|V_g| \gg |V_{th}|$, increases the number of carriers in the inversion layer. Increase in the number of carriers requires larger drain voltage V_{ds} for the pinch-off to occur. As a result of this, the transistor would operate for a large variation of the drain to source voltages V_{ds} before the pinch-off occurs [Neil H. E. Weste & Kamran Eshraghian, p.45-50]. As long as $dL \ll L$, as shown in Figure 14, the device behaves as a long channel device. When dL is not much less than L , the device behaves as a short channel device.

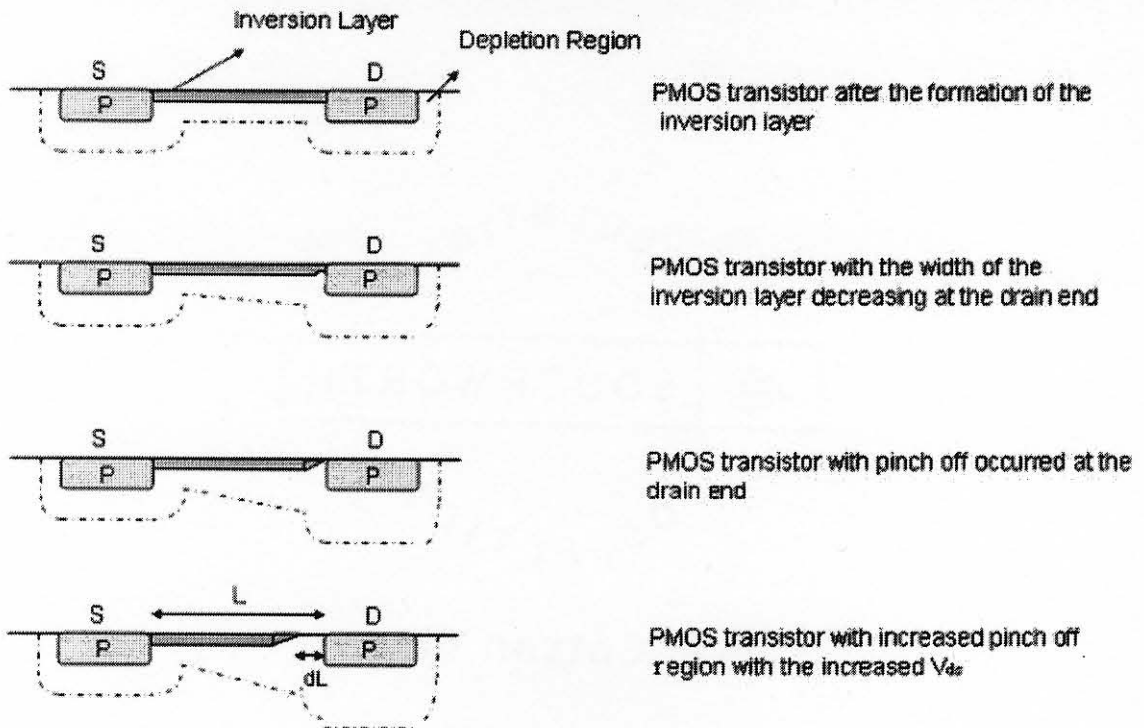


Figure 14 Different phases of the transistor operation with the regulation of V_{ds}

[Robert F. Pierret, p.67]

2.2.7 I-V Characteristics

I-V curves give the relation between the drain to source voltages (V_{ds}), drain current (I_{ds}) and the variation in these values with the varying gate voltage (V_g). The source is considered to be grounded. As the gate voltage increases, carriers at the interface increase. This reduces the drain to source voltage V_{ds} that is the turn on voltage. This causes an increase in the current as shown in Figure 15. Figure 16 can be used to determine the threshold voltage practically by graphing the relationship between the gate voltage and the drain current when the threshold voltage is very low and is difficult to observe. Else, the voltage at which

the channel starts conducting is the threshold voltage [Ben G Streetman & Sanjay Banerjee, p.290].

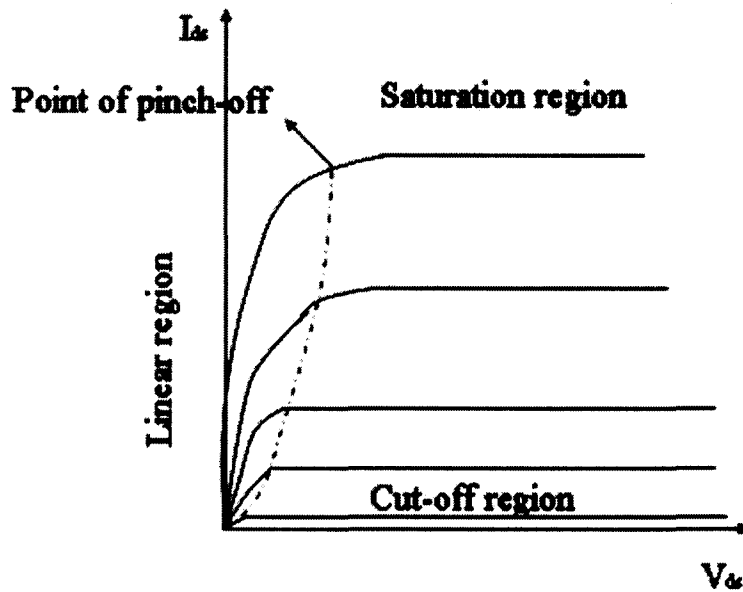


Figure 15 I-V curves for varying drain voltage and gate voltage [Robert F. Pierret, p.69]

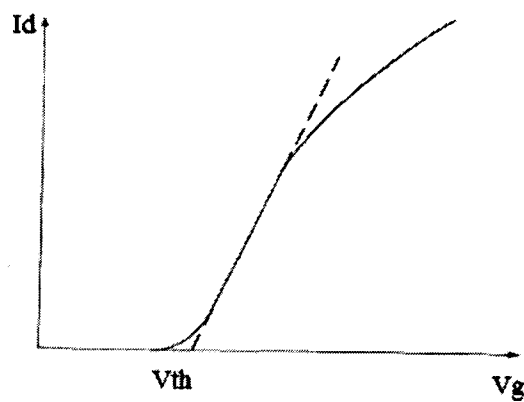


Figure 16 V_g Vs (I_d) for determining the threshold voltage V_{th} [Ben G Streetman & Sanjay Banerjee, p.290]

2.2.8 Interface biasing conditions

Positive or negative bias applied between the gate and the substrate results in varying the properties of the region at the Si-SiO₂ interface. Positive voltage results in accumulation region at the interface. Negative voltage results in depletion region initially and as the voltage increases it will result in the inversion region. The resulting band and charge diagrams and the type of regions at the Si-SiO₂ interface are explained below for n-type semiconductors.

2.2.8.1 Accumulation Region

Concentration of the majority carriers at the Si-SiO₂ interface is greater than the background concentration (N_b). The interface layer is accumulated with electrons. Concentration of the carriers at the interface depends on the bias V_g applied across the gate. The gate is positively biased with respect to the semiconductor. So, the semiconductor is at a negative potential. (The semiconductor Fermi energy level of the semiconductor rises to a higher energy level as $E = (-v) * (-q) = v * q$)

The positive bias results in a positive charge on the metal surface. This charge attracts negative charges in the semiconductor to the interface to compensate these positive charges. Fermi energy level is fixed relative to the conduction and the valence band energy levels. Increase in the concentration of the electrons at the interface results in bending the semiconductor valence and the conduction bands. In this state as the electron concentration increases, the conduction band needs to be closer to the Fermi level, so the bands bend in the

downward direction at the interface as shown in Figure 17a. Charge distribution on the metal plate is ($+Q$) and that on the semiconductor is ($-Q$).

Band bending and the position of the Fermi energy level of the metal relative to the semiconductor explained above causes the electrons to flow from the semiconductor to the Si-SiO₂ interface region. This causes accumulation of the electrons and the region is known as the accumulation region [Robert F. Pierret, p.34, Richard. C. Jaeger, p.117].

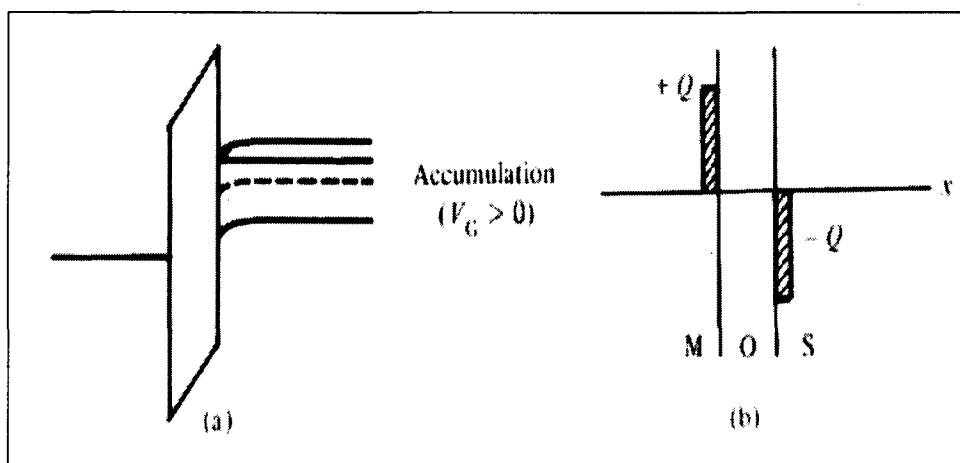


Figure 17a Energy band diagram and block charge diagram during accumulation [Robert F. Pierret, p.35]

2.2.8.2 Depletion Region

The Si-SiO₂ interface region depleted of majority carriers is known as the depletion region. The gate is negatively biased relative to the semiconductor. So, the semiconductor is at positive potential. (The semiconductor Fermi energy level lowers as $E = -q\phi$) The negative bias results a negative charge on the metal surface. This charge repels the majority carrier's electrons from the interface and

results in the depletion of the interface. This negative charge is compensated by the minority carriers, which attract towards the interface.

In this state, the electron concentration decreases resulting in bending the semiconductor valence and the conduction bands in the upward direction as shown in Figure 17b. Charge distribution on the metal plate is ($-Q$) and that on the semiconductor is ($+Q$) as shown in Figure 17b [Robert F. Pierret, p.34, Richard. C. Jaeger, p.117].

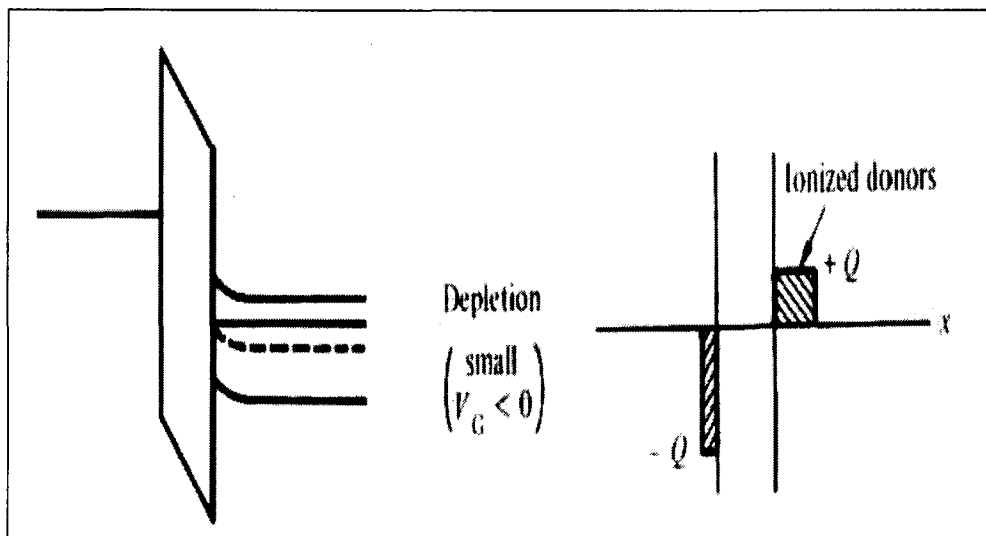


Figure 17b Energy band diagram and block charge diagram during depletion [Robert F. Pierret, p.35]

2.2.8.3 Inversion Region

The Si-SiO₂ interface region piled up of minority carriers is known as the inversion. Negative bias applied across the gate is more than the applied bias in case of the depletion region. Concentration of minority carriers at the interface equals to or greater than the background concentration N_b . So, the semiconductor is at positive potential. (The semiconductor Fermi energy level lowers as $E = -q\phi$)

Negative bias results in a negative charge on the metal surface. This negative charge repels the majority carrier's electrons from the interface and results in the depletion region. This negative charge is compensated by the minority carriers. The positive charges at the interface increase further in this case. This results in greater band bending in the semiconductor in the upward direction. This causes the intrinsic level to cross the Fermi level as shown in Figure 17c. The interface is said to be at the onset of the inversion.

If the negative bias is increased further, the concentration of the minority carriers at the interface is greater than the background concentration. The interface is at inversion as shown in Figure 17d. This bias is known as the threshold voltage. Charge distribution on the metal plate is ($-Q$) and that on the semiconductor is ($+Q$) [Robert F. Pierret, p.34, Richard. C. Jaeger, p.117].

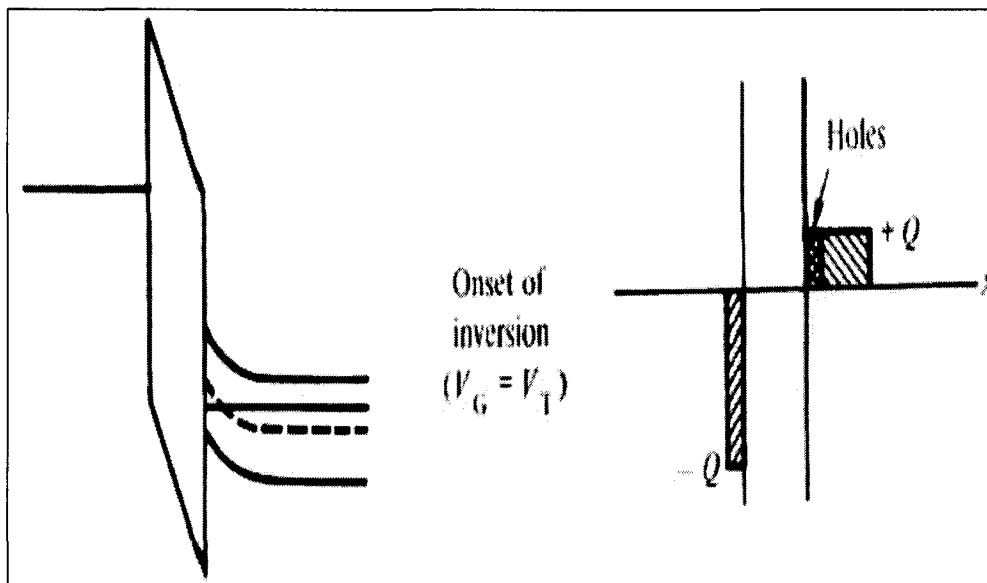


Figure 17c Energy band diagram and block charge diagram during the onset of inversion [Robert F. Pierret p.35]

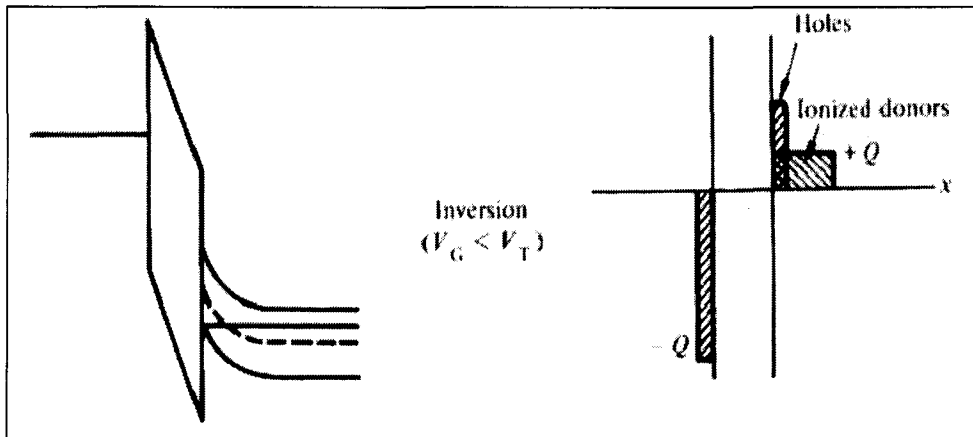


Figure 17d Energy band diagram and block charge diagram during inversion

[Robert F. Pierret, p.35]

2.2.9 PN-junction

PN-junctions exist on either side of the MOS-capacitor. PN-junction on the drain end of the channel must be reversed biased at all the times so that only a small leakage current flows through the diode into the semiconductor and the gate oxide. The source end of the channel is considered grounded. Generally the leakage current is ignored since leakage current $\ll I_d$. If the pn-junctions are forward biased they would result in a large forward current apart from the drain current which would flow through the semiconductor. This would result in improper performance of the transistor [Ben G Streetman & Sanjay Banerjee, p.145, Lloyd P. Hunter]

2.2.10 Test Structures

We have several test structures on the wafers which were fabricated. Resistors, Van der Pauw's structure, Kelvin structure and transistors include these test structures. Resistors are used to measure the resistance of the diffused regions, the Van der Pauw structure is used for measuring the sheet resistance, the Kelvin structure is used to measure the contact resistance, and the transistors are used to measure the transistor characteristics. Each of these structures will be explained in detail in upcoming sections.

2.2.10.1 Resistor

For a given voltage applied across the resistor the current passing through the resistor changes, thereby resulting in a measured resistance. Characteristics of the resistor are given by the I-V curves. Resistors are used to determine the type of contact between the metal and the semiconductor that is if the contacts are ohmic or rectifying contacts. Ohmic and rectifying contacts are explained in Section 2.2.9. Ohmic contacts are required as it results in low resistance. I-V characteristics pass through the origin. The resistor fabricated is shown in Figure 18.

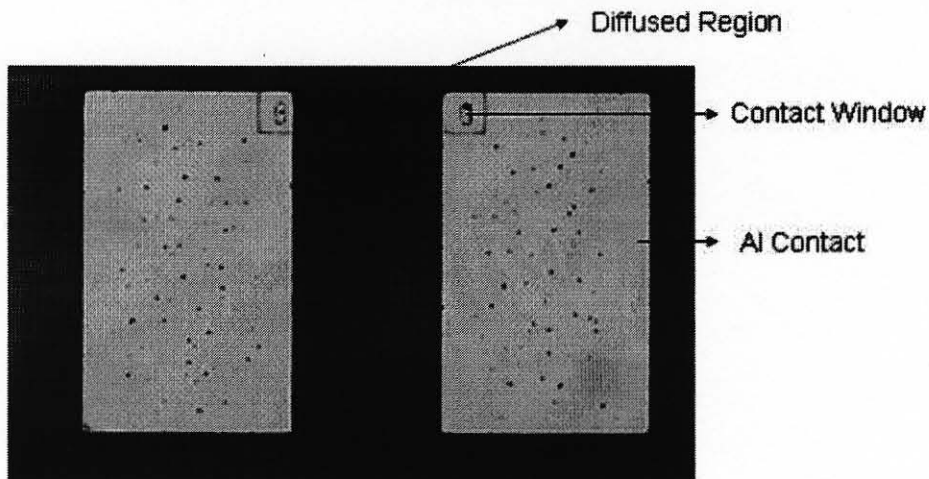


Figure 18 Resistor

2.2.10.2 Van der Pauw Structure

The Van der Pauw structure is used for determining the sheet resistance of a given sample or diffused region. Calculation of the sheet resistance is done by dividing the given sample into a number of equal squares and the resistance per number of squares gives the sheet resistance [Richard C. Jaeger, p.67]. The Van der Pauw structure is a symmetrical four-point structure that allows one to accurately determine sheet resistance without precisely knowing the number of squares in the device. Sheet resistance is measured in Ω/\square . The Van der Pauw structure we fabricated is shown in Figure 19.

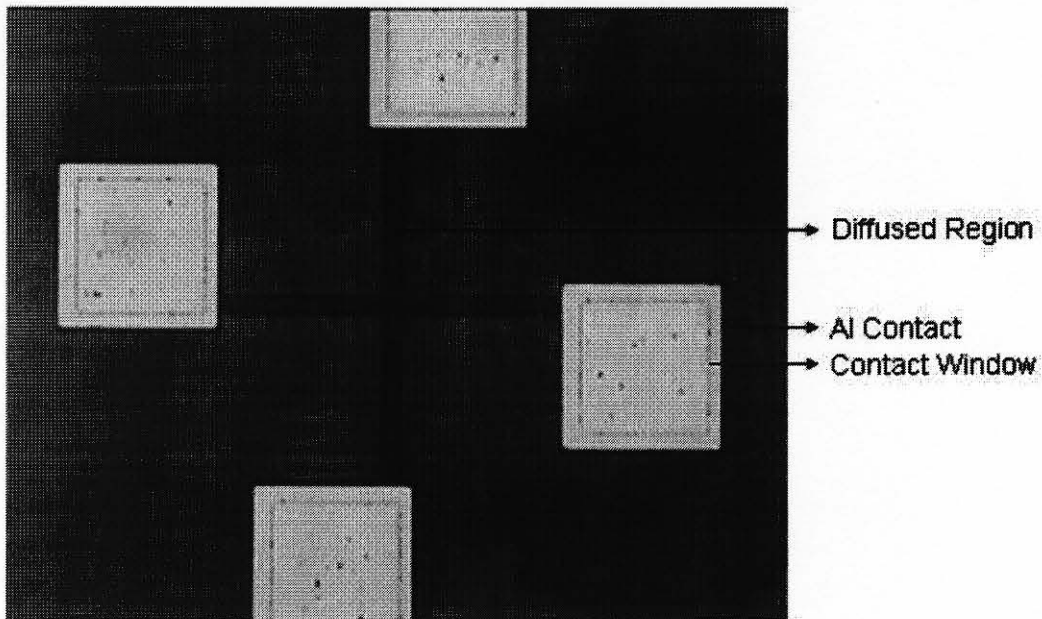


Figure 19 Van der Pauw structure

2.2.10.3 Cross Bridge Kelvin Resistor

The Cross bridge Kelvin structure can be used to determine contact resistance and resistivity. It is also known as a four terminal resistance measurement method. Importance of cross bridge Kelvin structure is to obtain low contact resistance. As the dimensions of the test structures increases, contact resistance decreases and vice versa. A low value of contact resistance is most desirable and the Cross Bridge Kelvin resistor fabricated is shown in Figure 20.

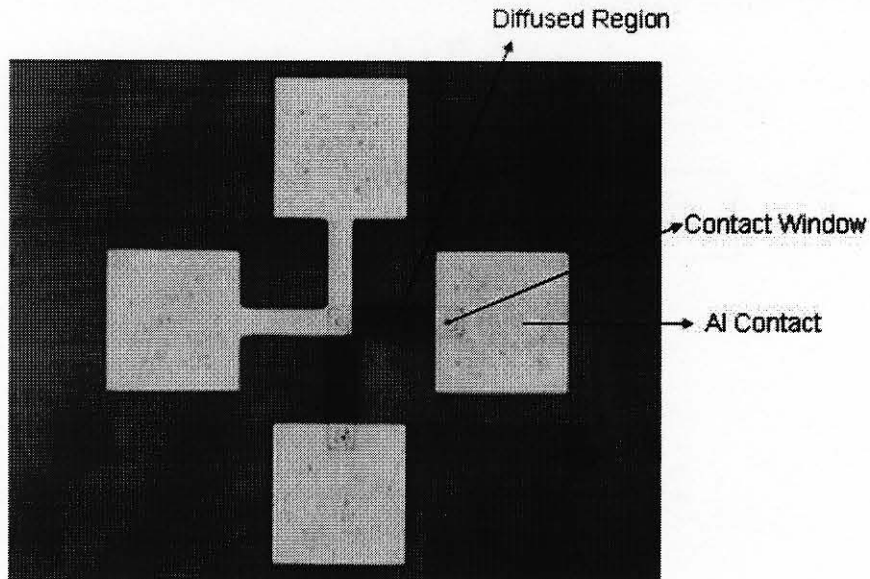


Figure 20 Cross Bridge Kelvin structure

2.2.10.4 Transistor

Theory of the transistors is explained in detailed in Section 2.2.5 and Section 2.2.6. The transistor fabricated is shown in Figure 21. A cross section of the figure is shown in Figure 26.

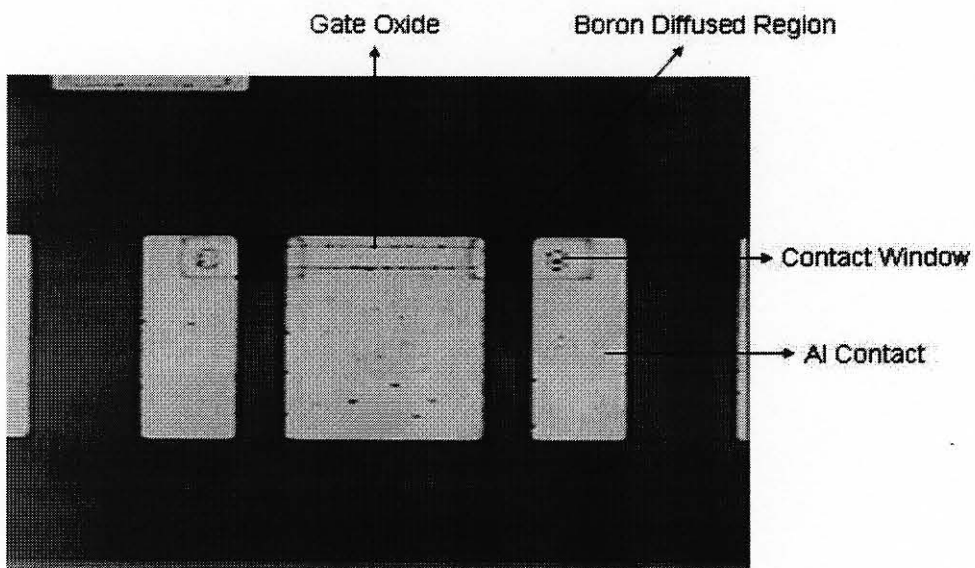


Figure 21 PMOS transistor

Chapter III

FABRICATION

This chapter explains the fabrication of the PMOS transistors and test structures. An overview of the fabrication sequences appears in Figure 26. Details of each individual process appear below.

3.1 Wafer characteristics

Table 2 N-type Wafer Characteristics

Wafer thickness	396um
Resistivity	5.39 Ω -cm
Sheet Resistance	1.36 $\times 10^2 \Omega$ /sqr

Characteristics of the wafers fabricated are given in the Table 2. Sheet resistance and resistivity mentioned in the Table 2 are measured using a Veeco four point probe instrument.

3.2 Wafer cleaning

Base clean and acid clean are done in order to remove organic, ionic and metallic contamination. Components of base clean and acid clean are H₂O:H₂O₂:NH₄OH and H₂O:H₂O₂: HCl respectively in the ratio of 5:1:1. Water and ammonium hydroxide or hydrochloric acid are mixed in the required ratio and heated to a temperature of 75°C on

the hotplate. Later hydrogen peroxide is added to the solution and the wafers are placed in the bubbling solution. About 10 minutes later the beaker is placed under running water and later the wafers are dried.

3.3 Oxidation

Plain wafers are wet oxidized to grow an oxide layer which acts as the masking layer for boron diffusion. The furnace is programmed for the settings given in Table 3. Nitrogen gas is turned ON for uniform heating of the furnace. The water in the bubbler is heated to a temperature of about 94°C. When the furnace reaches a temperature of about 950°C and water in the bubbler reaches a temperature of about 94°C, nitrogen is turned off and oxygen is passed through the bubbler and then the wafers are loaded into the furnace. The oxidized wafers are unloaded from the furnace. The oxide thickness is measured using the Filmetrics or system of the color chart. The temperature vs time graph for the furnace (temperature vs time) is shown in Figure 22.

Table 3 Oxidation furnace settings

Representation	Time/Temperature	Programmed value
P _{r1}	Ramp up temperature	20°C/minute
P ₁₁	Dwell temperature	1000°C
P _{d1}	Dwell time	1hr
P _{r2}	Ramp down temperature	20°C/minute
P ₁₂	Final temperature	350°C

Silicon reacts with oxygen in the furnace to form SiO_2 . SiO_2 thickness above the original surface of the wafer is $0.54X_o$ and $0.46X_o$ below the surface of the wafer where X_o is the oxide thickness. Oxide grown on the surface due to wet oxidation is not as dense as a dry oxide, so after 1 hour of wet oxidation the bubbler is turned OFF and dry oxidation takes place. One of the students loading the wafers into the furnace for the oxidation process is shown in Figure 23.

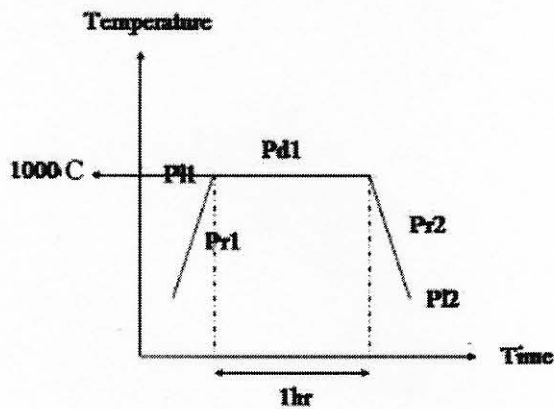


Figure 22 Temperature vs Time graph for the furnace

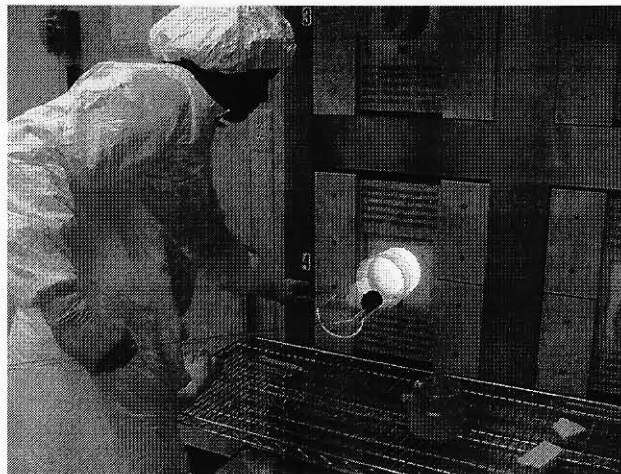


Figure 23 Student loading the wafers into the oxidation furnace

3.4 Photolithography

The oxidized wafers are cleaned using nitrogen gas. Shipley HMDS primer is spun on the wafer which improves the adhesion of the photoresist on the wafer. Shipley 1813 positive photoresist is spun on the wafer. The spinner settings are given in Table 4. The wafers are soft baked on a hot plate at 115°C for 75sec. Soft bake increases the adhesion of the photoresist and also dries any moisture on the surface of the wafer. The wafer is then loaded on the mask aligner for patterning. The wafer is aligned with the mask and then brought in contact with the mask. The wafer is exposed for 1.7 seconds. Alignment marks used for aligning the wafer with the mask are shown in Figure 24

Table 4 Spinner settings

Spread speed	400RPM	2 sec
Spin speed	4000RPM	10 sec

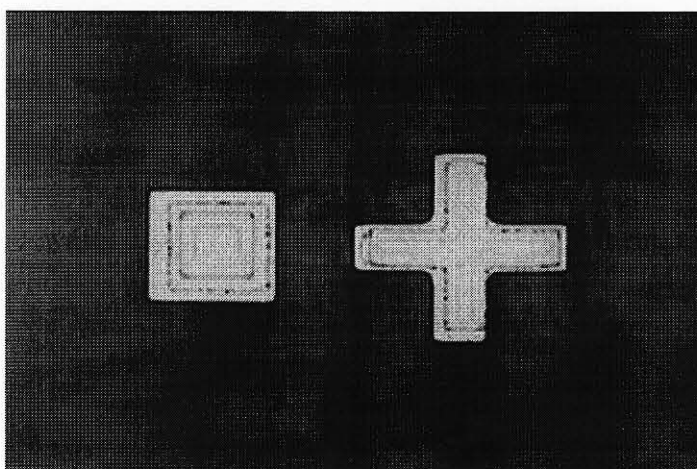


Figure 24 Alignment marks

The wafers are then developed in Microposit MF 319 (Metal Ion Free) for 45 seconds and rinsed under running water to remove the exposed photoresist and dried. Wafers are then examined under the microscope and then hard baked for about 4 to 5 minutes at 115°C. This improves the adhesion of the photoresist on the wafer so that the photoresist does not come off during the Buffer Oxide Etch (BOE).

BOE is done to etch the oxide from the regions where boron diffusion is to be done. BOE is done for about 4-5 minutes depending on the oxide thickness (etch rate 100nm/min) until the surface of silicon is hydrophobic. The wafers are then rinsed under running water and dried. In order to remove the photoresist, the wafers are rinsed with acetone and dried. Wafers are then nano-stripped to remove the residue due to the acetone and any photoresist left unresolved by the acetone. The wafers are then rinsed in water dried. Nano-strip leaves a thin layer of residual oxide. A slight 40:1 BOE is done to remove this thin layer of oxide.

3.5 Diffusion

Boron diffusion is done in order to create pn-junctions. Boron diffusion is done in two successive steps: Constant Source Diffusion followed by Limited Source Diffusion/Oxidation. Spin on boron PBF 20 is used as the source for boron diffusion. It is spun on the wafer at 4000RPM for 10sec. Respiratory filters are used while spinning the boron dopant as it is carcinogenic. The wafer is hard baked for 5 min at 200°C on the hot plate. The diffusion furnace settings are given in Table 5.

The gases used for boron diffusion are nitrogen and 3% O₂ in N₂. Nitrogen is used for maintaining the heat uniformly through out the furnace. As the furnace starts ramping up the wafers are loaded into the furnace. When the temperature reaches 1000°C, 3% O₂ in N₂ is passed through the furnace along with nitrogen. After 20 minutes of diffusion, nitrogen is stopped and only oxygen is passed through the furnace. This oxidation is done in order to create better variation in the heights of the structures, so that the features could be viewed clearly after the BOE.

Table 5 Diffusion furnace settings

Representation	Time/Temperature	Programmed value
P _{r1}	Ramp up temperature	20°C/minute
P _{l1}	Due temperature	1000°C
P _{d1}	Due time	1/2hr
P _{r2}	Ramp down temperature	20°C/minute
P _{l2}	Final temperature	350°C

BOE (6:1) is done in order to remove the borosilicate glass and oxide layer on the wafer. When it is observed that silicon is hydrophobic BOE is completed. The wafers are then rinsed under running water and dried. The diffusion performed is constant source diffusion.

Limited source diffusion acts a drive-in step and simultaneously grows a thin layer of oxide, which acts as the field oxide. The oxidation furnace settings are similar to the settings in Table 4 except the dwell time P_{d1} which is ½ hour.

The oxidation procedure is explained in Section 3.3. Limited source diffusion is also known as a drive-in step because it diffuses the boron further into the wafer.

3.6 Gate oxide windows

Procedure for opening windows for growing the gate oxide is similar to the procedure explained in Section 3.4. One of the students performing the lithography is shown in Figure 25.

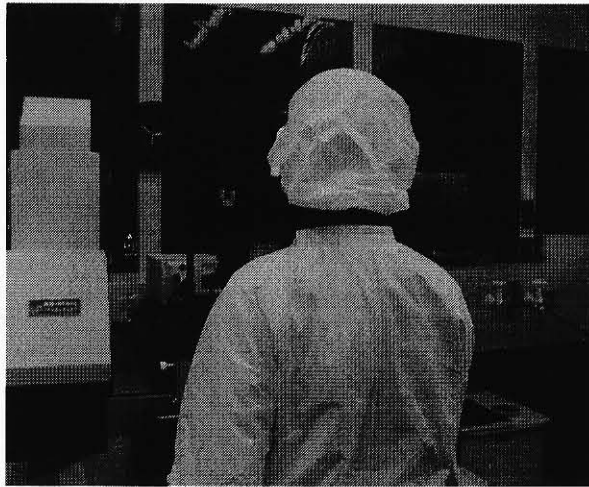


Figure 25 A student performing Lithography

3.7 Gate oxidation

Dry oxidation, wet oxidation and RTP processes were performed on the wafers for growing the gate oxide. The wet oxidation procedure is similar to the one explained in Section 3.3 except for the dwell time which is 10 minutes in this case. Drops of HCl are put in the bubbler to neutralize the oxide charges during the oxidation process. This process is known as the chlorine neutralization process. The dry oxidation process is similar to the wet oxidation process except

the dwell time which is 30-45 minutes. In case of RTP, the gate oxide is grown at a temperature of 1150°C for 2 minutes. Gate oxide grown using this process is considered to be free of mobile ions.

3.8 Photolithography

The oxidized wafers are patterned as explained in Section 3.4 for opening the contact windows for. The only difference is that, localized BOE is performed on one side of the wafer so that the oxide on the back side of the wafer could act as a masking layer during DRIE in case pressure sensors are to be fabricated.

3.9 Metallization

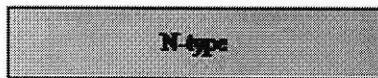
Pure aluminum is sputtered in order to make contacts and bonding pads. There are two types of sputtering mechanisms sputtering up and sputtering down. We use sputtering up mechanism that is the wafers are above the target. The sputtering machine can perform RF and DC sputtering. Metals and dielectrics are sputtered on RF side and on DC side only metals are sputtered. Argon is used in order to create the plasma because of the ability of the argon ions to move very fast and bombard with the aluminum target, thereby releasing aluminum ions in the upward direction to deposit on the surface of the wafer.

Initially sputtering must be done for a few seconds with the wafer not above the target to prevent sputtering of native oxide onto the wafer. Sputtering is done for 15 minutes with power 300 watts and base pressure 5.5×10^{-5} Torr. The

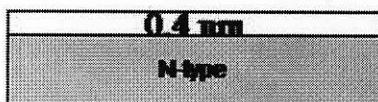
pressure gauge must be turned off when we start sputtering. Detailed start up procedure for the sputtering machine is given in the Appendix B.

3.10 Photolithography

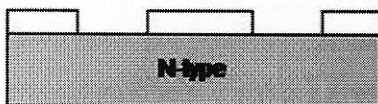
Metallized wafers are patterned as explained in the Section 3.4. Aluminum etchant is heated to 40°C so that it accelerates the etching process. The wafers are then placed in the etchant until the aluminum is etched. The wafers are then rinsed in water and dried. After the Nano-strip is done, the wafers must not be cleaned directly under the running water. Nano-strip has sulphuric acid in it which will strip the aluminum if placed under running water. Steps for the fabrication are shown in Figure 26.



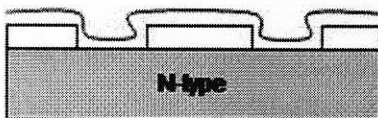
(100) n-type Silicon wafer



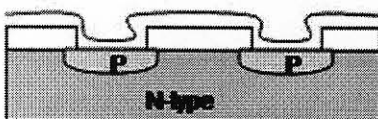
Wet oxidized silicon wafer



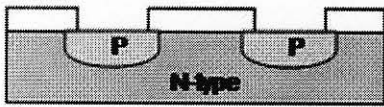
Photolithography for boron diffusion



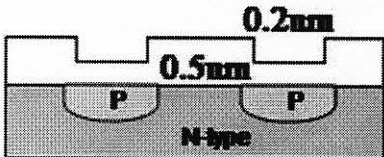
Spin-On boron dopant film



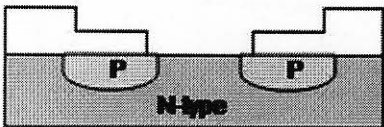
Constant source diffusion/pre-deposition at 1000° C, 30 minutes with N₂/O₂



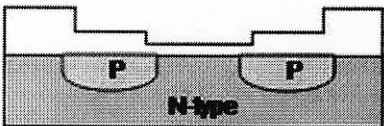
Borosilicate glass removed using BOE



Drive-in step/ Wet oxidation at 1000°C for 30 minutes



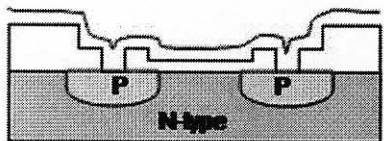
Photolithography for gate oxidation



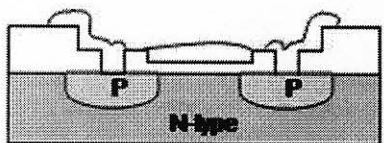
Gate oxidation using RTP/wet oxidation /dry oxidation



Photolithography for contact windows



Sputtering ≈ 0.2 nm Aluminum



Photolithography for making metal contacts

Figure 26 Steps for fabricating PMOS transistors

3.11 Annealing

Annealing is done in order to make good ohmic contact and to reduce the contact resistance. If there is a thin layer of oxide between the contact metal and silicon, contact resistance measured would be very high. To overcome this, annealing is done in an atmosphere of argon at 450°C for 15 minutes [Richard C. Jaeger]. The wafers are loaded into the furnace when it is cold and unloaded after the furnace cools down to prevent oxidation of the wafer which might result in high resistance. Annealing processes are explained in Section 2.2.4.2.

Chapter IV

TESTING & RESULTS

4.1 Resistor

For testing, electrical contact is made to the resistor using a probe station and the probe station is connected to a curve tracer. A variable voltage is applied across the resistor and the resultant current is shown on the curve tracer. Resistance is calculated using Equation 6. The average resistor values for dry oxidation, wet oxidation and RTP varies between 400Ω to 750Ω . The contact between the metal and the semiconductor is ohmic and is shown in Figure 27. Time and temperature variations for dry oxidation, wet oxidation and RTP are given in Table 6.

$$R = \frac{V}{I} \quad (6)$$

R= Ohmic resistance of the resistor (Ω)

V= Voltage applied across the resistor (volts)

I= current passing through the resistor (ampere)

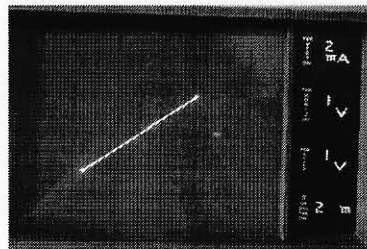


Figure 27 I-V curve of a resistor

Table 6 Conditions for different oxidation processes

	Dry Oxidation	Wet Oxidation	RTP
Time (min)	30-60	10	2
Temperature(°C)	1000	1000	1150
Thickness (nm)	60-120	120-130	40-60

4.2 Cross Bridge Kelvin structure

Electrical contact is made to the Cross Bridge Kelvin structure using the probe station. Current is forced to pass through one pair of opposite contact pads and the voltage is measured across the other pair of contacts as shown in Figure 28. In reality there is no current flowing through the second pair of contacts. The voltage drop across the contact at the center of the Cross Bridge Kelvin structure is the reason for the voltage measured across the other pair of contacts. Contact resistance is calculated using the Equation 7. Average values for contact resistance, for dry oxidation, wet oxidation and RTP, for the conditions given in Table 6 varies between 4.2Ω to 180Ω .

$$R_c = \frac{V_{ac}}{I_{bd}} \quad (7)$$

V_{ac} =Voltage measured between the contacts A and C (volts)

I_{bd} =Current applied between the contacts B and D (amps)

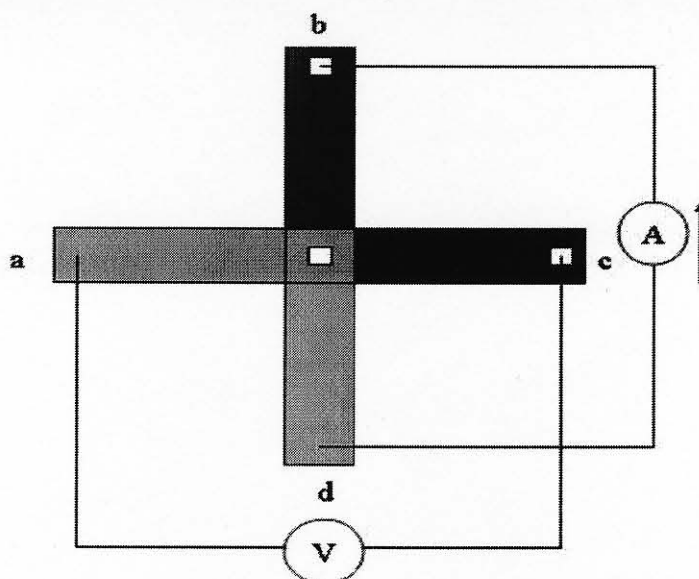


Figure 28 Contacts made to Cross Bridge Kelvin structure

4.3 Van Der Pauw Structure

Contacts are made to the Van der Pauw structure using the probe station. Current is passed through the adjacent pair of contacts and voltage is measured across the other pair of contacts for the structure shown in Figure 29. The resistance measured is known as the sheet resistance. Sheet resistance is calculated using the Equation 8 [Richard C.Jaeger]. Average values for sheet resistance, for dry oxidation, wet oxidation and RTP for the conditions given in Table 6 varies between $34.6 \Omega/\square$ to $4.5 \text{ K } \Omega/\square$.

$$R_s = 4.53 \times \frac{V_{cd}}{I_{ab}} \quad (8)$$

R_s = Sheet resistance (Ω/sqr)

I = Current injected across adjacent contacts (amps)

V = Voltage measured across adjacent contacts (volts)

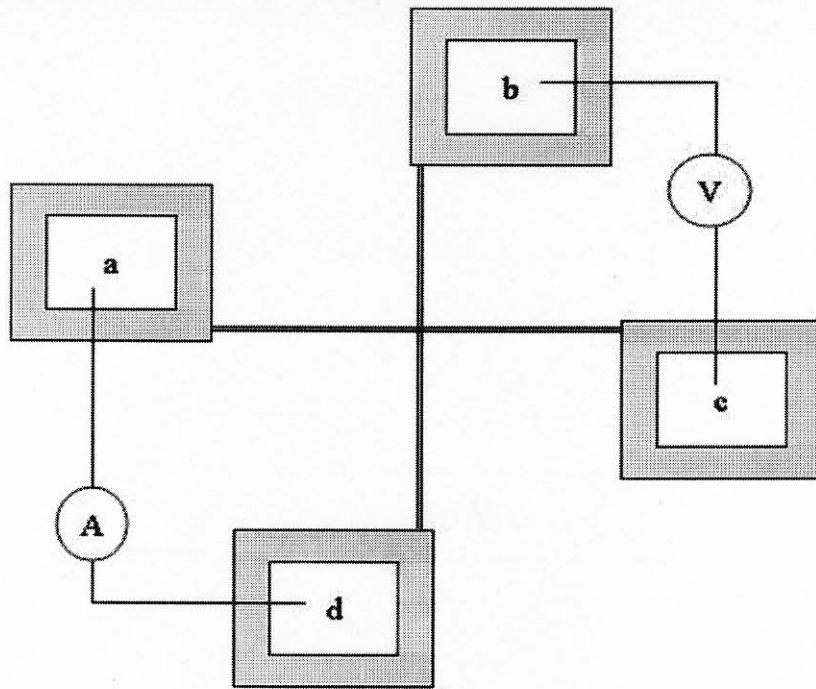


Figure 29 Contacts to the Van der Pauw structure

4.4 PMOS transistors

The PMOS transistor has three contacts (drain, source and gate) which are connected to the probe station as shown in Figure 30. The probe station in turn is connected to emitter, gate and collector of the curve tracer. The source is grounded and the gate and drain to source voltages are applied to the transistor. Appropriate settings are made on the curve tracer. The transistor is turned ON and the transistor characteristics are shown on the curve tracer. From the resultant curves, the transistor turn on voltage can be determined as explained in Section 2.2.3. Figure 31 shows contacts made to the wafer using the probe station. General characteristics for a PMOS transistor are shown in Figure 32.

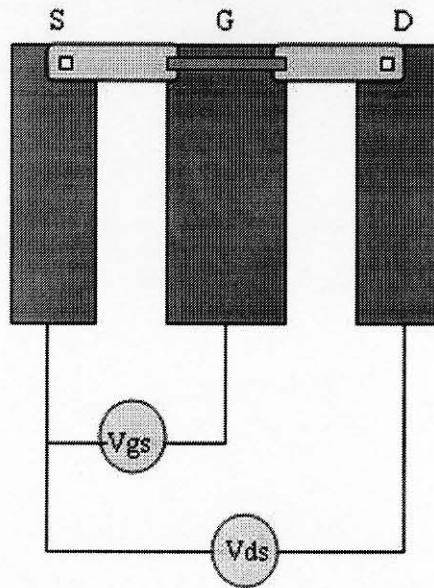


Figure 30 Contacts to the transistor

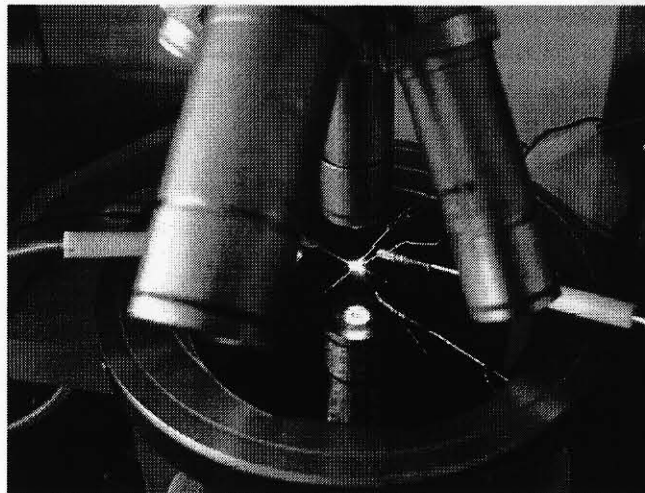


Figure 31 Contacts made to the transistor using the probe station

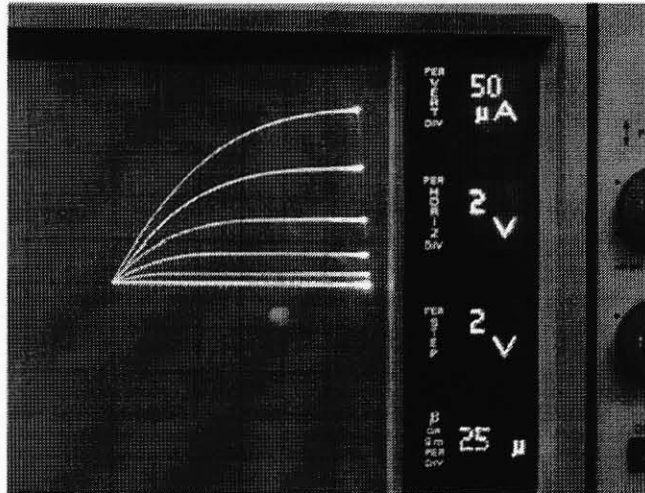


Figure 32 PMOS transistor characteristics

Varying threshold voltage for varying gate oxides grown using dry oxidation, wet oxidation and rapid thermal processing are given in Table 7 and the graph is given in Figure 33. Figure 33 shows that V_{th} (wet oxidation) $>$ V_{th} (dry oxidation) $>$ V_{th} (RTP). From the experimental and theoretical threshold voltage it is observed that V_{th} (theoretical) $>$ V_{th} (experimental). For example $V_{th} = 2.585$ volts (theoretical value of dry oxidation) $>$ $V_{th}=2$ volts (experimental value of dry oxidation).

Varying threshold voltage for gate oxide grown and oxide grown during the diffusion process acting as the gate oxide are given in Table 8 and the graph is shown in Figure 34. Figure 34 shows that V_{th} (oxide from diffusion) $>$ V_{th} (gate oxide grown).

Table 7 Data for different oxidation processes

Dry Oxidation $t_{ox}=60nm$		Wet Oxidation $t_{ox}=130nm$		RTP $t_{ox}=30nm$	
V_{gs} (volts)	I_{ds} (μA)	V_{gs} (volts)	I_{ds} (μA)	V_{gs} (volts)	I_{ds} (μA)
1	0	2	0	1	10
2	2	4	1	2	20
3	8	6	8	3	50
4	20	8	22		
5	35	10	50		
6	52	12	88		

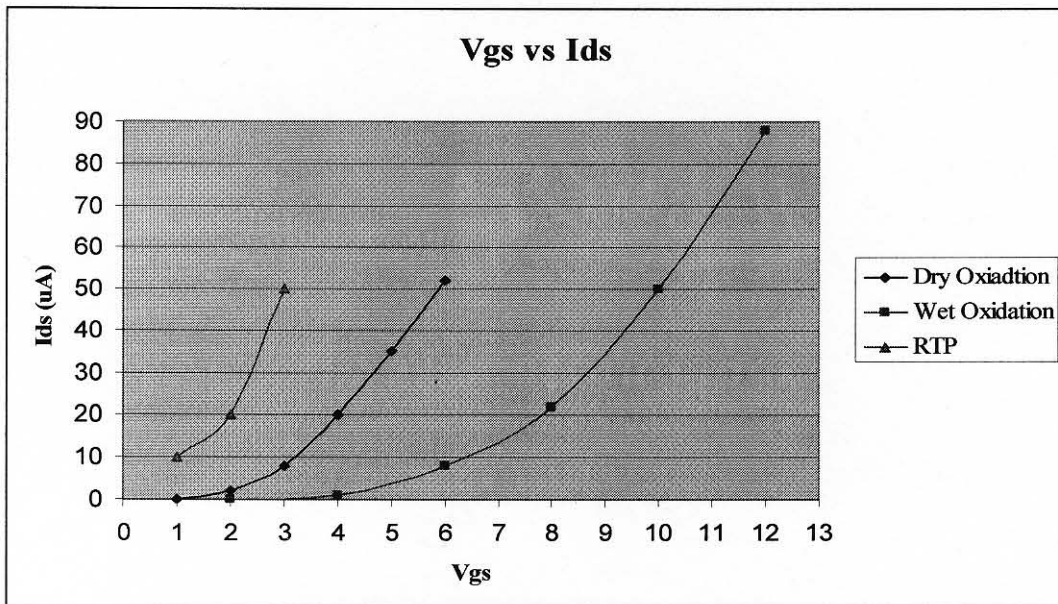


Figure 33 V_{gs} vs I_{ds} for different oxidation processes

Table 8 Data for gate oxide grown separately and oxide grown during the limited source diffusion acting as the gate oxide

Gate Oxide Grown $t_{ox}=40\text{nm}$ (RTP)		Oxide Grown during Diffusion acts as Gate Oxide $t_{ox}=200\text{nm}$	
V_{gs} (volts)	I_{ds} (μA)	V_{gs} (volts)	I_{ds} (μA)
2	0	2	0
4	2	4	0
6	8	6	0
8	26	8	8
10	50	10	24
12	80	12	50

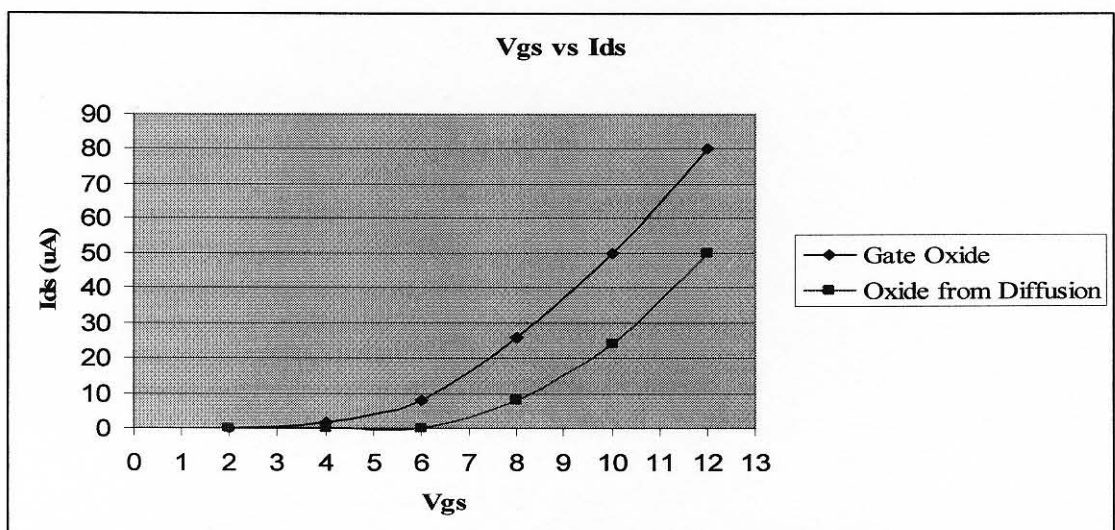


Figure 34 V_{gs} vs I_{ds} for gate oxide grown and oxide grown during diffusion

Chapter V

CONCLUSIONS AND RECOMMENDATIONS

A basic operating procedure of the PMOS transistors, the importance of the threshold voltage, pinch-off voltage and their dependence on the gate oxide thickness has been presented. Also, three different processes have been employed for growing the gate oxide and their experimental and theoretical values of voltages have been compared. Measurement of MOS capacitance and C-V characterization is recommended. This will determine the presence of oxide charges in the gate oxide. Fabrication methods can be varied depending on the type of gate material, oxide thickness and type of insulator required.

Results accomplished from the process of fabrication of the PMOS transistors are:

- 1) The fabrication can be done either by using 3 masks or a 4 mask process.
- 2) Fabrication of the transistor and importance of gate oxide has been explained in detail, characterized and documented.
- 3) Wet oxidation with drops of HCl in the bubbler has been employed to reduce the mobile charges in the gate oxide.
- 4) Probable effect of the temperature of the surroundings has been noticed on the performance of the transistors.
- 5) Experimental and theoretical values are compared, which seems appropriate.

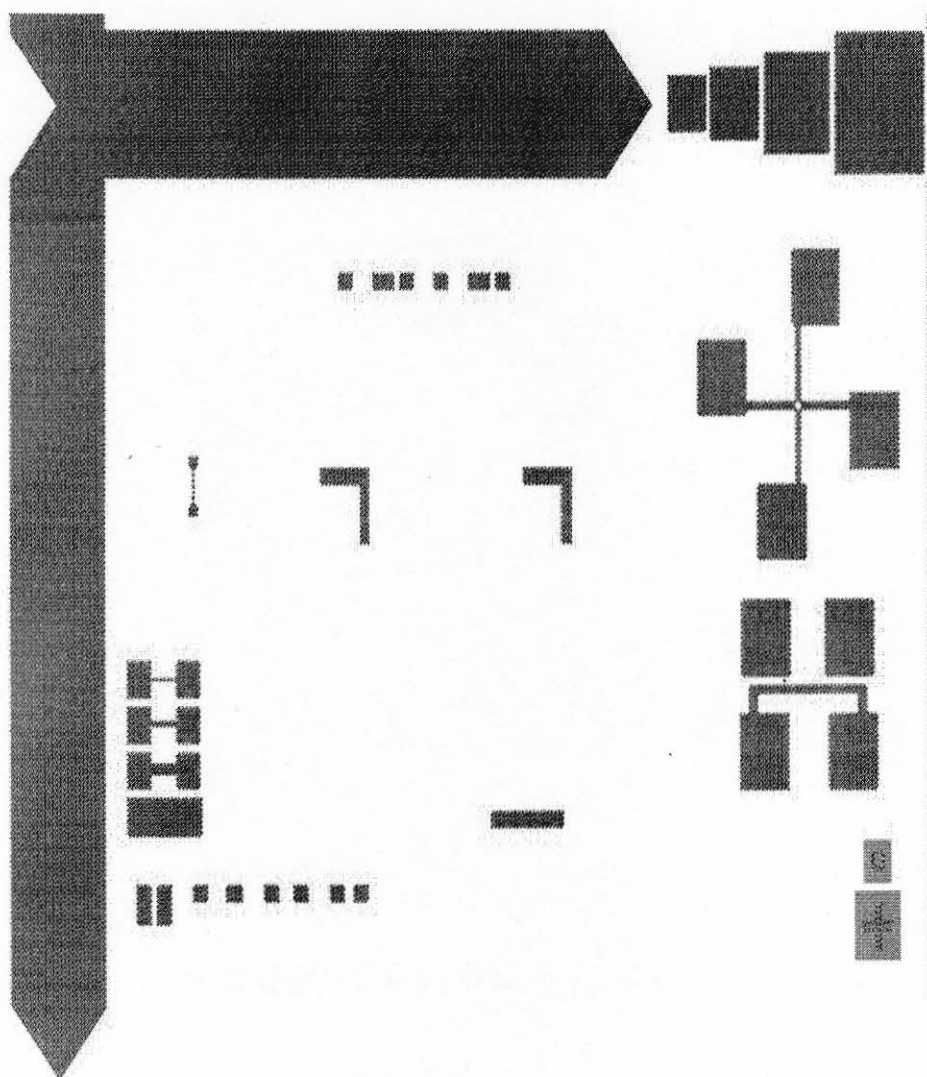
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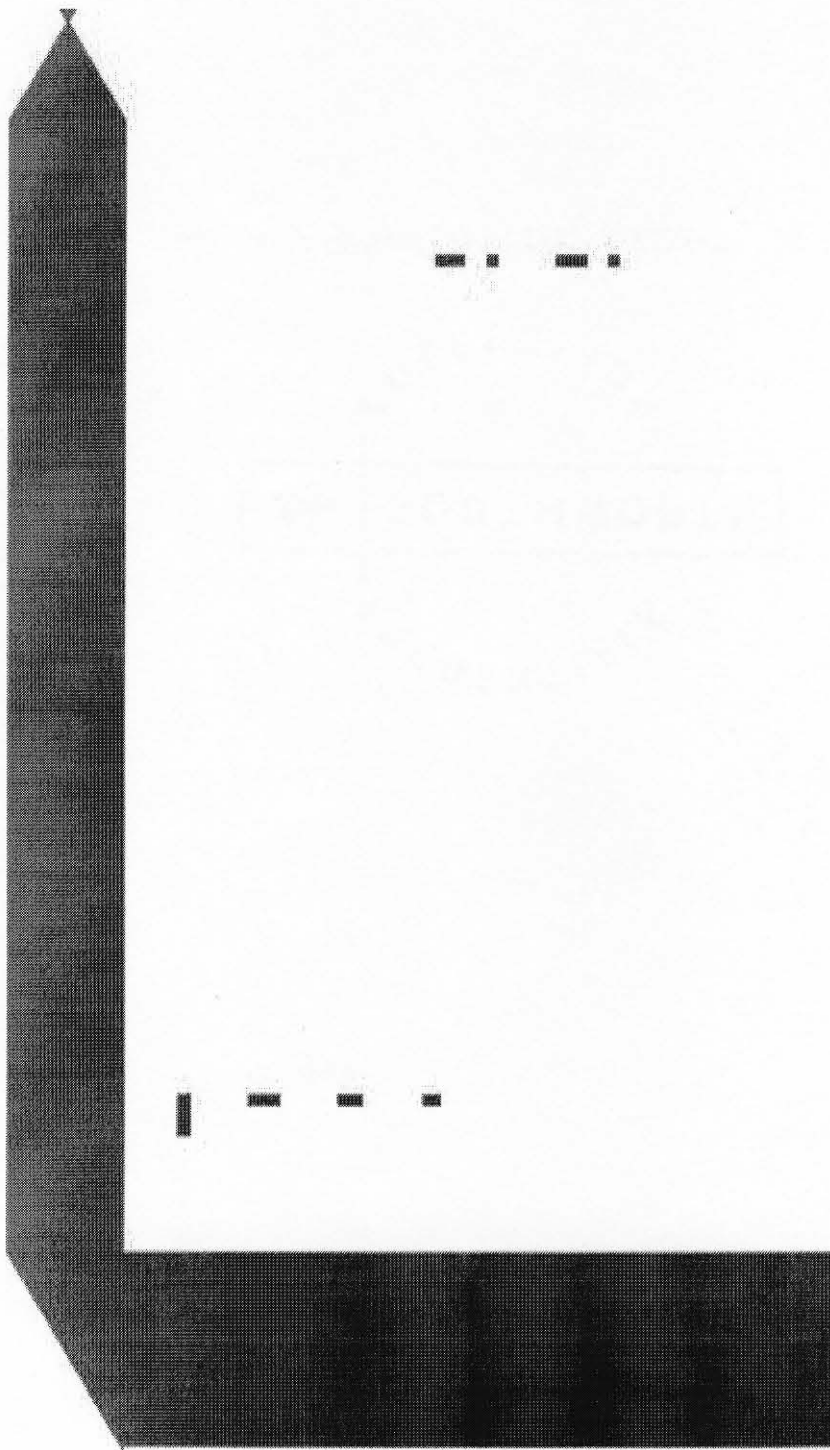
APPENDIX A

MASKS

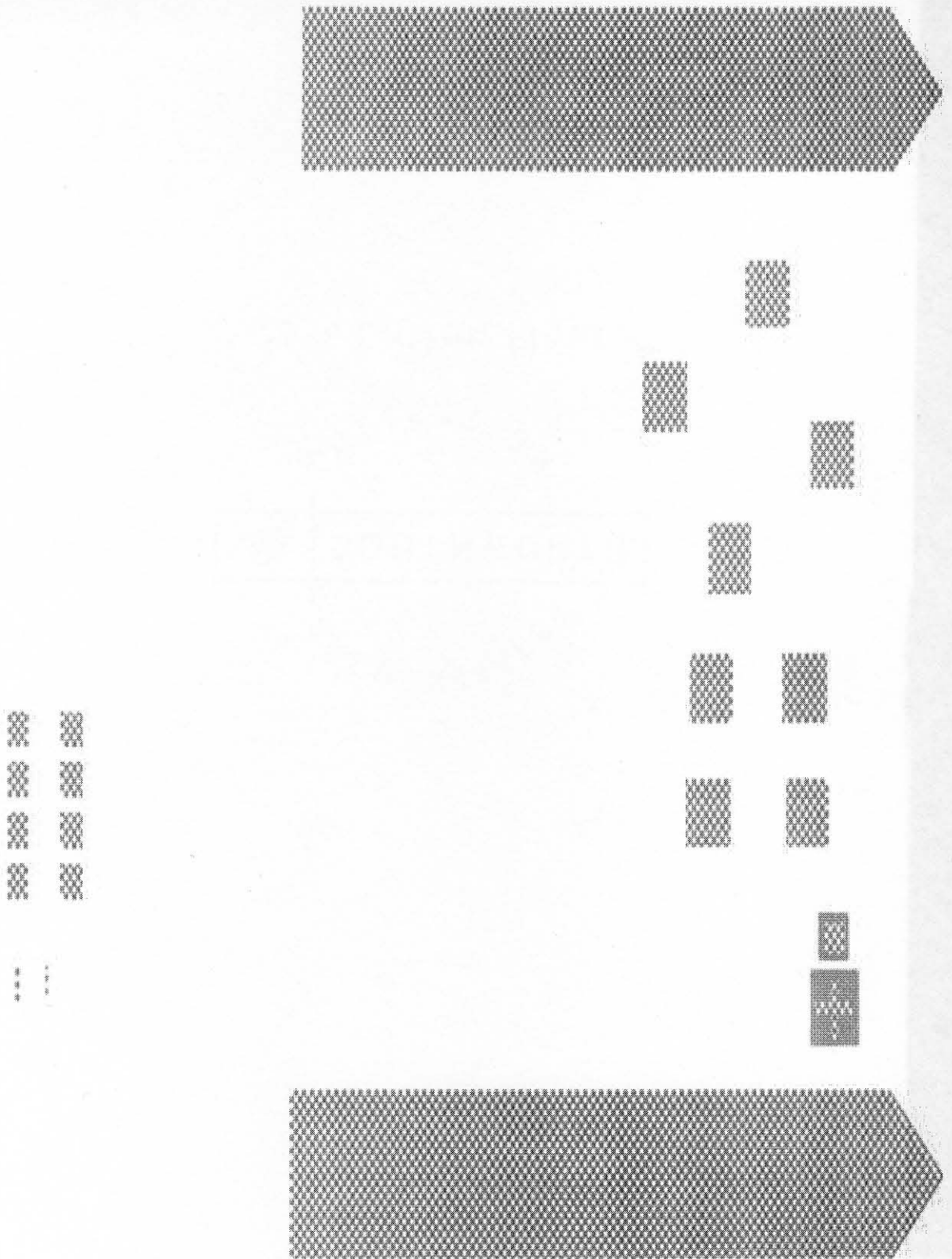
Masks for the fabrication of the transistors and the test structures are shown below. The fabrication process involves four lithographic processes for boron diffusion, gate oxide growth, opening contact windows and metal patterning.



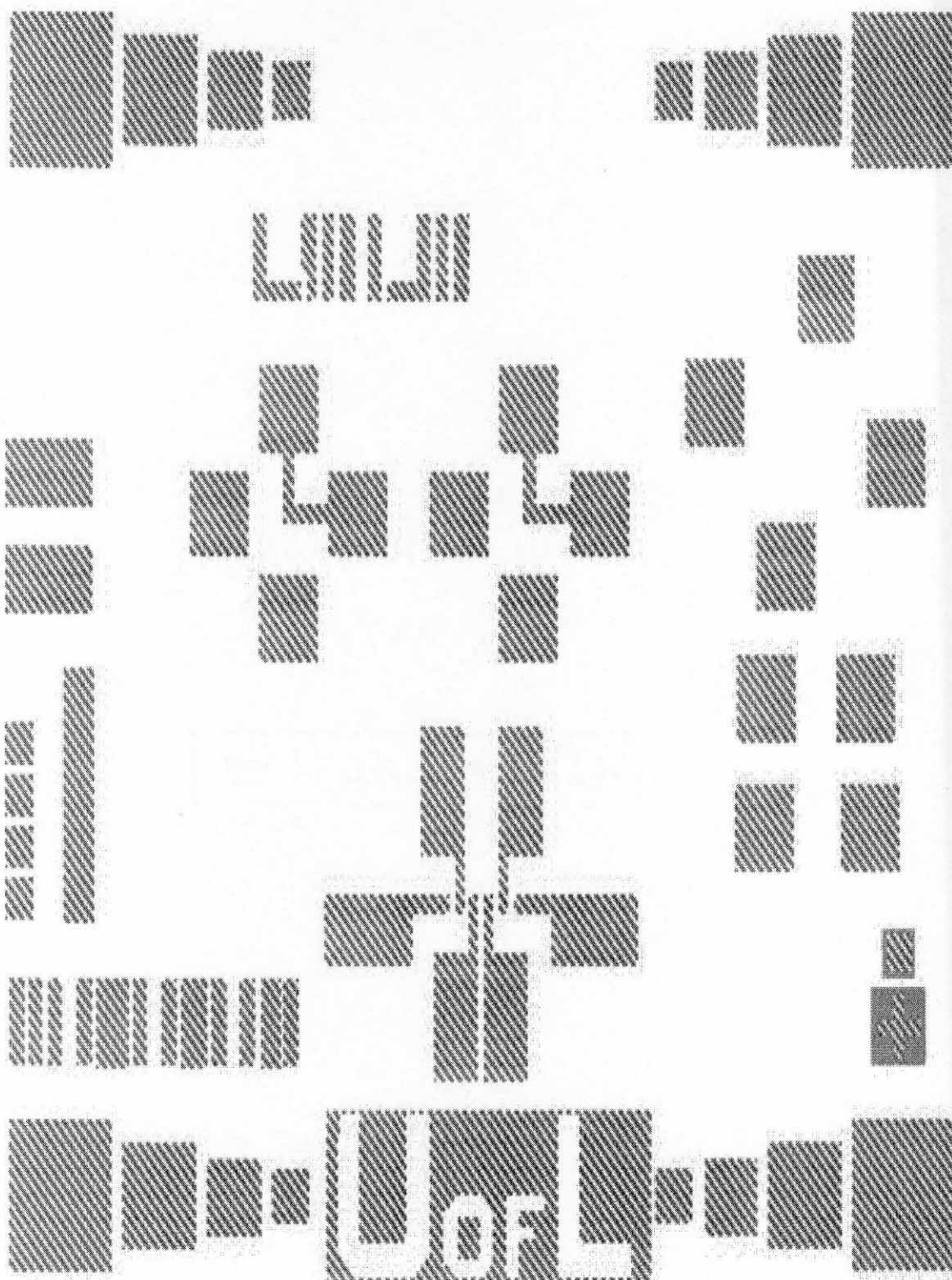
Mask for boron diffusion



Mask for Opening Windows for Growing Gate Oxide



Mask for opening contact windows



Mask for patterning the metal

THRESHOLD VOLTAGE CALCULATIONS

Variables	Voltage Drops	Threshold Voltage	
$\epsilon_s := 104.477 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}$	Permittivity of Silicon	$N_d := 10^{15} \text{ cm}^{-3}$	Background Concentration
$\epsilon_{ox} := 34.530 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}$	Permittivity of Oxide	$t_{ox} := 0.06 \cdot 10^{-4} \text{ cm}$	Gate Oxide Thickness [Variable]
$q := 1.6 \cdot 10^{-19} \text{ C}$	Electron Charge	$k := 1.38 \cdot 10^{-23} \frac{\text{J}}{\text{K}}$	Boltzman Constant
$n_i := 1.5 \cdot 10^{10} \text{ cm}^{-3}$	Intrinsic Concentration	$T := 300 \text{ K}$	Temperature
$\frac{k \cdot T}{q} = 0.026 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$			
$.025875000000000000000000 \cdot \frac{\text{J}}{\text{C}}$			
$k \cdot T \cdot \frac{\ln\left(\frac{N_d}{n_i}\right)}{q} = 0.287 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$		$\phi_f := k \cdot T \cdot \frac{\ln\left(\frac{N_d}{n_i}\right)}{q}$	Barrier Height
$.28740553673380590699 \cdot \frac{\text{J}}{\text{C}}$			
$\frac{\epsilon_{ox}}{t_{ox}} = 5.755 \cdot 10^{-4} \cdot \text{kg}^{-1} \cdot \text{m}^{-4} \cdot \text{s}^4 \cdot \text{A}^2$		$C_{ox} := \frac{\epsilon_{ox}}{t_{ox}}$	Gate oxide Capacitance
$5.7550000000000000000000 \cdot 10^{-8} \cdot \frac{\text{F}}{\text{cm}^2}$			
$\frac{\sqrt{4 \cdot \epsilon_s \cdot q \cdot N_d \cdot \phi_f}}{C_{ox}} = 0.241 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$		$V_{td} := \frac{\sqrt{4 \cdot \epsilon_s \cdot q \cdot N_d \cdot \phi_f}}{C_{ox}}$	Voltage Drop across the Gate Oxide
$.24088101416911026907 \cdot \sqrt{\frac{\text{F}}{\text{cm}^4}} \cdot \frac{\text{J}}{\text{F}} \cdot \text{cm}^2$			
$\phi_f \cdot 2 = 0.575 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$		$\phi_s := \phi_f \cdot 2$	Voltage required for inversion
$.57481107346761181398 \cdot \frac{\text{J}}{\text{C}}$			

$$V_{id} - \phi_s + V_{ox} = 2.585 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1} \quad V_{th} = V_{id} - \phi_s + V_{ox} \quad \text{Threshold Voltage}$$

Wet Oxidation

Variables

Voltage Drops

Threshold Voltage

$\epsilon_s := 104.477 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}$ $\epsilon_{ox} := 34.530 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}$ $q := 1.6 \cdot 10^{-19} \text{ C}$ $n_i := 1.5 \cdot 10^{10} \text{ cm}^{-3}$ $\frac{k \cdot T}{q} = 0.026 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$ $.025875000000000000000000 \cdot \frac{\text{J}}{\text{C}}$ $k \cdot T \cdot \frac{\ln\left(\frac{N_d}{n_i}\right)}{q} = 0.287 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$ $.28740553673380590699 \cdot \frac{\text{J}}{\text{C}}$ $\frac{\epsilon_{ox}}{\text{tox}} = 2.466 \cdot 10^{-4} \cdot \text{kg}^{-1} \cdot \text{m}^{-4} \cdot \text{s}^4 \cdot \text{A}^2$ $5.7550000000000000000000 \cdot 10^{-8} \cdot \frac{\text{F}}{\text{cm}^2}$ $\frac{\sqrt{4 \cdot \epsilon_s \cdot q \cdot N_d \cdot \phi_f}}{C_{ox}} = 0.562 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$ $.24088101416911026907 \cdot \sqrt{\frac{\text{F}}{\text{cm}^4} \cdot \frac{\text{J}}{\text{F}}} \cdot \text{cm}^2$ $\phi_f/2 = 0.575 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$ $.57481107346761181398 \cdot \frac{\text{J}}{\text{C}}$	$\text{Permittivity of Silicon}$ $\text{Permittivity of Oxide}$ Electron Charge $\text{Intrinsic Concentration}$ $T := 300 \text{ K}$ Barrier Height $C_{ox} := \frac{\epsilon_{ox}}{\text{tox}}$ $\text{Gate oxide Capacitance}$ $V_{id} = \frac{\sqrt{4 \cdot \epsilon_s \cdot q \cdot N_d \cdot \phi_f}}{C_{ox}}$ $\text{Voltage Drop across the Gate Oxide}$ $\phi_s := \phi_f/2$ $\text{Voltage required for inversion}$	$N_d := 10^{15} \text{ cm}^{-3}$ $\text{Background Concentration}$ $\text{tox} := 0.14 \cdot 10^{-4} \text{ cm}$ $\text{Gate Oxide Thickness [Variable]}$ $k := 1.38 \cdot 10^{-23} \frac{\text{J}}{\text{K}}$ Boltzman Constant Temperature
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Consider the Charges in the Gate Oxide to be the Constant Values given below

$Q_f := 5 \cdot 10^{10} \text{ cm}^{-2}$ $Q_m := 0 \text{ cm}^{-2}$ $Q_{ot} := 0 \text{ cm}^{-2}$ $Q_{it} := 10^{12} \text{ cm}^{-2}$ $Q_{tot} := Q_f + Q_m + Q_{ot} + Q_{it}$ $Q_{tot} = 1.05 \cdot 10^{16} \cdot \text{m}^{-2}$ $10500000000000000000000000 \cdot \text{cm}^2$ $q \cdot \frac{Q_{tot}}{C_{ox}} = 6.811 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$ $2.9192006950477845352 \cdot \frac{\text{C}}{\text{F}}$	Fixed Charge Mobile Charge Oxide Trap Charge $\text{Interfacial Trap Charge}$ Total charge $V_{ox} := q \cdot \frac{Q_{tot}}{C_{ox}}$ $\text{Voltage Drop Due to the Charges in the Oxide}$	$V_{th} := V_{id} - \phi_s + V_{ox}$ Threshold Voltage
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RTP

Variables

Voltage Drops

Threshold Voltage

$$\begin{aligned} ss &:= 104.477 \cdot 10^{-14} \frac{\text{F}}{\text{cm}} & \text{Permittivity of Silicon} & Nd := 10^{15} \text{ cm}^{-3} & \text{Background Concentration} \\ sox &:= 34.530 \cdot 10^{-14} \frac{\text{F}}{\text{cm}} & \text{Permittivity of Oxide} & tox := 0.04 \cdot 10^{-4} \text{ cm} & \text{Gate Oxide Thickness [Variable]} \\ q &:= 1.6 \cdot 10^{-19} \text{ C} & \text{Electron Charge} & k &:= 1.38 \cdot 10^{-23} \frac{\text{J}}{\text{K}} & \text{Boltzman Constant} \\ ni &:= 1.5 \cdot 10^{10} \text{ cm}^{-3} & \text{Intrinsic Concentration} & T &:= 300 \text{ K} & \text{Temperature} \\ \frac{k \cdot T}{q} &= 0.026 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1} \end{aligned}$$

$$0.025875000000000000000000 \cdot \frac{\text{J}}{\text{C}}$$

$$k \cdot T \cdot \frac{\ln\left(\frac{Nd}{ni}\right)}{q} = 0.287 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$$

$$287.40553673380590699 \cdot \frac{\text{J}}{\text{C}}$$

$$\phi_f := k \cdot T \cdot \frac{\ln\left(\frac{Nd}{ni}\right)}{q} \quad \text{Barrier Height}$$

$$\frac{sox}{tox} = 8.632 \cdot 10^{-4} \cdot \text{kg}^{-1} \cdot \text{m}^{-4} \cdot \text{s}^4 \cdot \text{A}^2$$

$$Cox := \frac{sox}{tox} \quad \text{Gate oxide Capacitance}$$

$$5.7550000000000000000000 \cdot 10^{-8} \cdot \frac{\text{F}}{\text{cm}^2}$$

$$\frac{\sqrt{4 \cdot ss \cdot q \cdot Nd \cdot \phi_f}}{Cox} = 0.161 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$$

$$V_{id} := \frac{\sqrt{4 \cdot ss \cdot q \cdot Nd \cdot \phi_f}}{Cox} \quad \text{Voltage Drop across the Gate Oxide}$$

$$24088101416911026907 \cdot \sqrt{\frac{\frac{\text{F}}{\text{cm}^4} \cdot \text{J}}{\text{F}}} \cdot \text{cm}^2$$

$$\phi_{f2} = 0.575 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$$

$$\phi_s := \phi_{f2} \quad \text{Voltage required for inversion}$$

$$57481107346761181398 \cdot \frac{\text{J}}{\text{C}}$$

Consider the Charges in the Gate Oxide to be the Constant Values given below

$$\begin{aligned} Q_f &:= 5 \cdot 10^{10} \text{ cm}^{-2} & \text{Fixed Charge} & Q_{ot} &:= 0 \text{ cm}^{-2} & \text{Oxide Trap Charge} \\ Q_m &:= 0 \text{ cm}^{-2} & \text{Mobile Charge} & Q_{it} &:= 10^{12} \text{ cm}^{-2} & \text{Interfacial Trap Charge} \end{aligned}$$

$$Q_f + Q_m + Q_{ot} + Q_{it} = 1.05 \cdot 10^{16} \cdot \text{m}^{-2}$$

$$10500000000000 \text{ cm}^2$$

$$Q_{tot} := Q_f + Q_m + Q_{ot} + Q_{it} \quad \text{Total charge}$$

$$q \cdot \frac{Q_{tot}}{Cox} = 1.946 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$$

$$V_{ox} := q \cdot \frac{Q_{tot}}{Cox} \quad \text{Voltage Drop Due to the Charges in the Oxide}$$

$$2.9192006950477845352 \cdot \frac{\text{C}}{\text{F}}$$

$$V_{id} - \phi_s + V_{ox} = 1.532 \cdot \text{kg} \cdot \text{m}^2 \cdot \text{s}^{-3} \cdot \text{A}^{-1}$$

$$V_{th} := V_{id} - \phi_s + V_{ox} \quad \text{Threshold Voltage}$$

APPENDIX C

SPUTTERING SOP

- 1) Sputtering is done for the deposition of the metal onto the silicon wafer. For sputtering the metal we use Technics RF/DC sputterer.
 - a. Turn ON the nitrogen (venting) and argon gas (sputter gas) valves.
 - b. Turn the chiller ON.
 - c. Turn ON the sputterer. Flip the vent toggle to ON state for venting the sputtering machine.
 - d. Place the required target and the wafer to be sputtered.
 - e. Close the shutter and open the roughing valve by flipping the toggle to ON position.
 - f. When the pressure goes below 100mTorr, flip the toggle to OFF position and flip the fore line toggle to ON position. Later turn ON the turbo pump.
 - g. When the turbo pump speed goes below 27000 RPM flip the gate valve toggle to ON position.
 - h. When the base pressure reaches 5.5×10^{-5} mTorr the system is ready for performing the sputtering. The pressure is seen in the pressure gauge.
 - i. Before starting to sputter, flip the pressure gauge toggle to OFF position.
 - j. It can be run either in auto or manual mode using RF or DC power.
 - k. Flip the toggle to auto mode and turn the argon gas. Flip the toggle to RF power. Set the required time, power and press the START switch. The metal gets deposited on the wafer.
 - l. For metals like aluminum, sputter with out the wafer on the top of the target so that if there is any oxide on the target it would not deposit on to the wafer.
 - m. Flip all the toggles (gate valve, fore line valve, turbo pump, argon gas) to OFF position. Flip the vent toggle to ON position and remove the wafers deposited with the metal.

- n. Close the chamber lid and shut down the system.

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